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Performance of Symmetrical and Asymmetrical Multilevel Inverters

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Abstract: Distributed Energy Resources (DER) are systems that produce electrical power at the site where the power is needed. If only electrical power is used then the technology is called Distributed Generation (DG). The objective of this paper is to study a novel more than five level multistring inverter topology for DERs based DC/AC conversion system. The distributed energy resource based single-phase inverter is usually adopted in the microgrid system. In order to reduce the conversion losses, the key is to saving costs and size by removing any kind of transformer as well as reducing the power switches. In this study, a high step-up converter is introduced as a front-end stage to improve the conversion efficiency of conventional boost converters and to stabilize the output DC voltage of various DERs such as photovoltaic for use with the simplified multilevel inverter. In addition, two active switches are operated under line frequency. In this project a novel asymmetrical configuration is proposed. The proposed asymmetrical configuration uses less number of switches to get more levels. It will reduce the cost, reduce the number of sources, complexity, losses and improves reliability. The proposed converter is simulated by Matlab/Simulink software and simulation results are presented.

Key words: DC/AC power conversion, multilevel inverter, harmonic analysis and Total Harmonic Distortion (THD).

I. INTRODUCTION

The continuous economic development of many countries and the environmental issues (gas emissions and the green house effect) observed in the last decades forced an intense research in renewable energy sources. Distributed energy resources are small, modular, energy generation and storage technologies that provide electric capacity or energy where you need it. Typically producing less than 10 megawatts (MW) of power, DER systems can usually be sized to meet your particular needs and installed on site.

DER technologies include wind turbines, photo voltaic (PV), fuel cells, micro turbines, reciprocating engines, Hydro, combustion turbines and energy storage systems are the most explored technologies due to their considerable advantages [1],[2], such as reliability, reasonable installation and energy production costs, low environmental impact, capability to support micro grid [3].

The renewable energy resources consists of photovoltaic, fuel cells are generate the voltage are dc voltage. But I want the ac voltage because of mostly used the loads are ac loads. So we are convert the dc power to ac powerprocessing interface is required and is Commercial, homes, factories and utility grid standards [4],[7].

Differing converter topographies have been acquired DERs establish effectual power flow control performance of DERs. DER systems may be either connected to the local electric power grid or isolated from the grid in stand-alone applications [7], [10].

The dc-dc converters are two types. They are without galvanic isolation and with galvanic isolation (high frequency transformer).The with galvanic isolation converter (high power applications) are used corresponding to size, weight, expense reduces. So low and medium power applications without galvanic isolation means make no use of transformers corresponding to reduces the size, weight expense [7], [8].

The next procedure the output voltage level increases of the inverter output then automatically harmonic component of the output voltage of inverter reduces and also corresponding to small size of filters are used simultaneously the cost reduces. The differing multilevel topographies are usually characterizing by strong reduction of switching power losses and electromagnetic interference (EMI) [6], [7], [8].

A new simplified single-phase multistring five-level multilevel inverter topography of dc/ac power conversion with auxiliary circuit proposed [8], [9]. This topography are used, the number of switching devices and output harmonics are reduced. The THD of the multistring five-level inverter is much less than the conventional multistring three-level inverter because of additional auxiliary circuit has high switching losses [9].

The objective of this paper is to study a newly constructed transformerless five level multistring inverter topology for DERS. In this letter aforesaid GZV-based inverter is reduced to a multistring multilevel inverter topography that require only 6 active switches instead of existing cascaded H-bridge multilevel inverter have eight switches[10].Multi string multilevel inverter have six active switches. They are middle two switches are operated fundamental frequency and remaining four switches are operated switching frequency. A high efficiency dc-dc boost converter reduction of transformer and device voltage and current stresses with continuous input current leakage inductance energy recovery, and avoiding the use of electrolytic capacitor due to reduced ripple current[13]. Operation of the system configuration of operation is shown below. The performance of symmetrical and asymmetrical single phase multilevel inverter with respect to harmonics content and number of switches and input voltage source is DC is simulated by MATLAB/Simulink. A detailed harmonic

analysis is done on the multilevel inverter by considering up to 23rd harmonics for 7 levels to 13 levels operation.

II. SYSTEM CONFIGURATION OF OPERATION PRINCIPLES

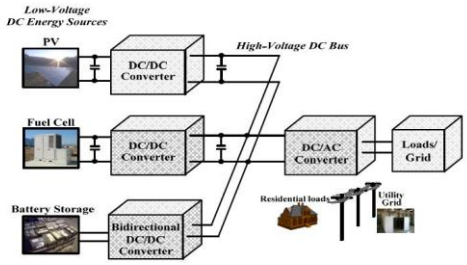


Fig.1 Different type of DERs are system configuration of Multistring Inverter

The above Fig.1 shows the DERs have photovoltaics or Fuel cell inverter are taken as [14].The individual dc/dc boost converter are connected to the photovoltaic modules or Fuel cell. The bidirectional (buck-boost) dc/dc converter is connected to the only for battery storage. The individual dc/dc boost converter is connected to the multistring inverter. These common inverter for interface with all dc/dc converters of DERs [15]. The two modes of operation above Fig.1. They are standalone mode and grid connected mode. In grid connected mode, the battery storage energy is not connected to the grid. In standalone operation, the battery storage energy is connected to the load.

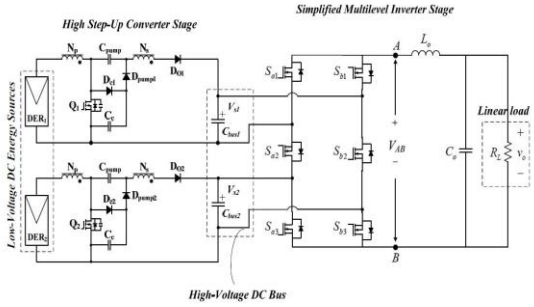


Fig.2 Single phase simplified multistring five-level inverter topography for high stepup converter from DERs

The above Fig.2 shows DER module-1 is connected to the high step up dc/dc converter and DER module-2 is connected to high step up dc/dc converter. These two converters are connected to their individual dc-bus capacitor and a simplified multilevel inverter. The resistive load is connected output of the simplified multilevel inverter from DER through high step up dc/dc converter. The input sources of DERs are photovoltaic or Fuel cells. The basic circuit have eight switches of cascaded H-bridge Multilevel inverter (CHB) with phase shift carrier pulse width modulation scheme are used. The simplified multilevel inverter have six switches then best merits of improved output waveforms, reduced the filter size, low EMI and THD [11],[12]. It should be noted that, by using independent voltage regulation control of the individual high step-up converter, voltage balance control for the two bus capacitors C_{bus1}, C_{bus2} can be achieved normally.

2.1. High Step-Up Converter Stage

In this study, High Efficiency Converter with Charge Pump and Coupled Inductor for Wide Input Photovoltaic AC Module Applications [13].This simplified multilevel inverter combines the behavior of three different converter topologies: boost, flyback and charge pump. The flyback aspect of the topology allows the design to be optimized in terms of the transformer turns-ratio, allowing for much higher voltage gains than would be possible with a boost converter. However, flyback converters are notoriously inefficient and are very sensitive to leakage inductance, which can cause undue voltage-stress on switches and diodes. By using a clamp-circuit- identical to the output of a boost-converter-after the main switch, much of the efficiency issues can be resolved and the transformer design becomes less complicated. Finally, adding a charge-pump capacitor across the primary and secondary windings of the transformers gives higher converter voltage-gain and reduced peak current stress by allowing the current of the primary-windings to continuous.

The equivalent circuit of the proposed converter is shown in Fig.3. The coupled inductor is modeled as a magnetizing inductor L_m an ideal transformer with a turn's ratio of $N_s : N_p$ primaryleakage inductor L_{Lk1} and secondary leakage inductor L_{Lk2}. C_c is the clamp capacitor, S is the Active switch, D_0 is the output diode C_{pump} is the charge pump capacitor.

According to voltage-seconds balance condition of the magnetizing inductor, the voltage of the primary winding can be derived as

$$\mathbf{V}_{\text{pri}} = \mathbf{V}_{\text{in}} \frac{\text{D}}{1-\text{D}} \qquad (1)$$

Where V_{in} represents each the low-voltage dc energy input sources and voltage of the secondary winding is

$$\mathbf{V}_{\text{sec}} = \frac{\mathbf{N}_{\text{S}}}{\mathbf{N}_{\text{P}}} \cdot \mathbf{V}_{\text{pri}} = \frac{\mathbf{N}_{\text{S}}}{\mathbf{N}_{\text{P}}} \cdot \mathbf{V}_{\text{in}} \frac{\text{D}}{1-\text{D}} \qquad (2)$$

Similar to that of the boost converter, the voltage of the charge-pump capacitor C_{pump} and clamp capacitor C_c can be expressed as

$$\mathbf{V}_{\text{C pump}} = \mathbf{V}_{\text{C c}} = \mathbf{V}_{\text{in}} \cdot \frac{1}{1-\text{D}} \qquad (3)$$

Hence, the voltage conversion ratio of the high step-up converter, named input voltage to bus voltage ratio, can be derived as [13].

$$\frac{\mathbf{V}_0}{\mathbf{V}_{\text{in}}} = \frac{\left(2 + \mathbf{N}_{\text{S}} \big/ \mathbf{N}_{\text{P}} . \text{D}\right)}{1-\text{D}} \qquad (4)$$

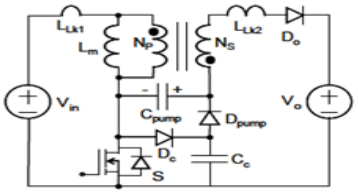


Fig.3. Equivalent circuit of the high step-up boost converter

2.2 Simplified Multilevel Inverter Stage

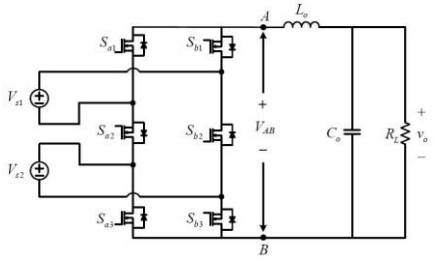


Fig.4 Basic Five-level inverter Circuitry of six switches

The simplified multilevel inverter is the conventional circuit of five level inverter Fig.4 shows above. A new single phase multistring topography, as a new basic circuitry in Fig.4.Referring to Fig.2, it is should assumed that, in this configuration, the two capacitors in the capacitive voltage divider are connected directly across the dc bus and all switching combinations are activated in an output cycle. The dynamic voltage balance between the two capacitors is automatically controlled by the preceding high step-up converter stage. Then, we can assume $V_{s1} = V_{s2} = V_s$.

This circuit has six power switches compare the basic circuit of cascaded H-bridge has eight power switches which drastically reduces the power circuit complexity and simplifies modulation circuit design and implementation. The phase disposition (PD) pulse width modulation (PWM) control scheme is introduced to generate switching signals and to produce five output voltage levels: $0, V_s, 2V_s, -V_s$ and $2V_s$

This inverter topology uses two carrier signals and one reference signal to generate the PWM signals for the switches the modulation strategy and its implemented logic scheme in Fig.5 (a) and (b) area widely used alternative for Phase disposition modulation. With the exception of an offset value equivalent to the carrier signal amplitude. Two comparators are used in this scheme with identical carrier signals V_{tri1} and V_{tri2} toprovidehigh–frequencyswitchingsignals for S_{a1}, S_{b1}, S_{a3} and S_{b3}. Another comparator is used for zero-crossing detection to provide line-frequency switching signals for switches S_{a2} and S_{b2}.

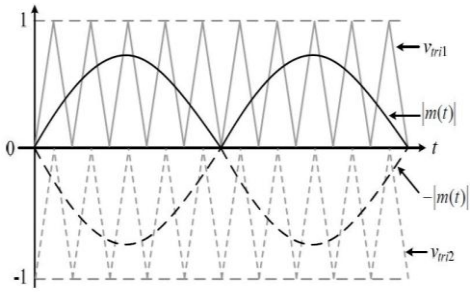
For Fig.4 the switching function of the switch defined as follows.

S_{aj} = **1**, S_{aj} ON

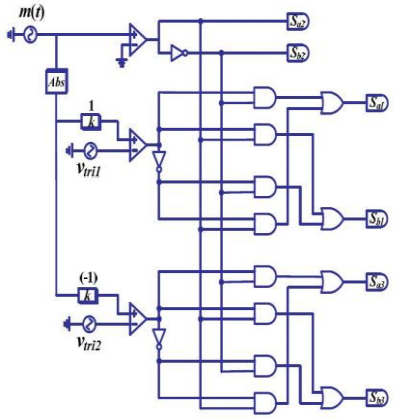
S_{aj} = **0**, S_{aj} OFF for j=**1, 2, 3**

S_{bj} = **1**, S_{bj} ON

S_{bj} = **0**, S_{bj} OFF for j=**1, 2, 3**



(a)



(b)

Fig.5. Modulation strategy a) Carrier/reference signals (b) modulation logic

Table-I
Simplified Five Level Inverter Switching Combination

S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}	V_{AB}
0	**1**	**0**	**1**	**0**	**1**	$2V_S$
0	**1**	**1**	**1**	**0**	**0**	V_S
1	**1**	**0**	**0**	**0**	**1**	V_S
1	**1**	**1**	**0**	**0**	**0**	**0**
0	**0**	**0**	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**	**1**	$-V_S$
0	**0**	**1**	**1**	**1**	**0**	$-V_S$
1	**0**	**1**	**0**	**1**	**0**	$-2V_S$

Table-I lists switching combinations that generate the required five output levels. The corresponding operation modes of the simplified multilevel inverter stage are described clearly as follows.

1) Maximum positive output voltage **($2V_S$)**: Active switches S_{a2}, S_{b3} and S_{b1} are ON. The voltage applied to the LC output filter is $2V_S$.

2) Half level positive output voltage ($+V_S$): The two switching combinations are there. One switching combination

is that active switches S_{a2}, S_{a3} and S_{b1} are ON, the other is active switches S_{a2}, S_{a1} and S_{b3} are ON. During this operating stage, the voltage applied to the LC output filter $+V_S$.

3) Zero Output, (0): This output condition either one of the leg are left or right all switches are ON. The load is short-circuited, and the voltage applied to the load terminals zero.

4) Half level negative output voltage $(-V_S)$: the two switching combinations are there. One switching combination is such that active switches S_{a1}, S_{b2} and S_{b3} are ON, the other switching is active switches S_{b2}, S_{b1} and S_{a3}.

5) Maximum negative output $(-2V_S)$: During this stage, active switches S_{a1}, S_{a3} and S_{b2} are ON, and the output voltage applied to the LC output filter $-2V_S$.

In these circuit operations, it can be observed that the open voltage stress of the active power switches S_{a1}, S_{b1}, S_{a3} and S_{b3} is equal to input voltage V_S and the main active switches S_{a2} and S_{b2} are operated at the line frequency. Hence, the switching losses are reduced in the new topology and the overall conversion efficiency is improved.

In Fig.5 control circuit diagram as shown, $m(t)$ is the sinusoidal modulation signal. Both V_{tri1} and V_{tri2} are two carrier signals. The magnitude value and frequency of the sinusoidal modulation signal are given as m_{peak}=0.7 and f_m=60Hz. The peak to peak value of the triangular modulation signals is equal to 1 and the switching frequency f_{tri1} and f_{tri2} are both given as 18.06 kHz.

The two input voltage sources feeding from the high step up converter is controlled at 100V that is $V_{s1} = V_{s2} = 100$V. The five level output of the phase voltage of the simulation waveform is shown in Fig.6.

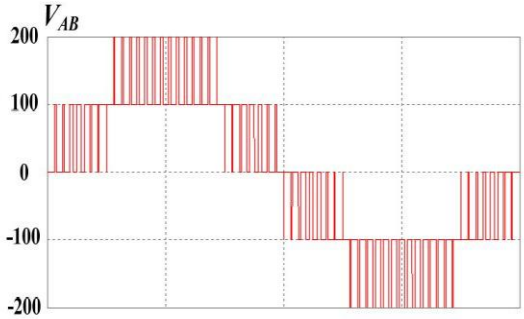


Fig.6 Simplified multilevel five level output phase voltage of simulation waveform V_{AB}

2.3 Basic circuit of Cascaded H-Bridge (CHB) Inverter

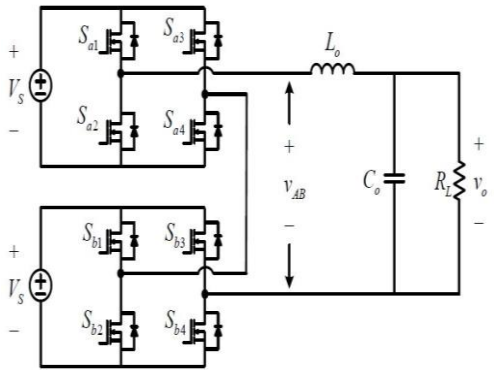


Fig.7 Basic circuit of five-level inverter topology of CHB inverter have eight switches

The above figure shows the Basic circuit of five level inverter CCHB inverter have eight switches. The carrier based sinusoidal phase shift carrier pulse width modulations are used in the basic circuit of CHB inverter. The eight switches are operated of the switching frequency. The CHB inverter are operate at the switching frequency is same as18.06kHz the same modulation index m_a=0.7.

The simplified multilevel inverter and Cascaded H-bridge inverter are operated the same switching frequency and same modulation index m_a,the same input voltage V_S=100V and output L-C filter, L_0=20mH, C_0=200uF, R-load =10Ohms. Table VII and Table VIII shows the harmonic component and THD Cascaded H-Bridge Inverter and Simplified multilevel inverter. The simplified multilevel inverter have the lesser THD compare to the Cascaded H-bridge inverter. So the low values of LC filter.

The symmetrical multilevel inverters are Cascaded H-bridge inverter and Simplified multilevel inverter. These are taken the equal voltage values. The symmetrical multilevel inverters above are operated with PWM method. The Proposing methods of asymmetrical multilevel inverters are repeating sequence is used for Seven, Nine, Eleven and Thirteen levels. The seven level have 6switches and Nine, Eleven and Thirteen level have 8 switches. The Seven, Nine, Eleven and Thirteen levels are get by using 12,16,20,24 switches are necessity in symmetrical configuration of Cascaded H-bridge inverter. So the less number of switches are in asymmetrical configuration to get more number of voltage levels, lesser the THD, low cost, reducing the DC sources, reduce the complexity and driving circuits.

III. PROPOSED SYTEM

3.1Seven Level Multi Level Inverter (MLI)

Table- II
Seven Level Multilevel Inverter (MLI)

S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}	V_0
0	1	0	1	0	1	$3V_S$
1	1	0	0	0	1	$2V_S$
0	1	1	1	0	0	V_S
1	1	1	0	0	0	0
0	0	0	1	1	1	0
1	0	0	0	1	1	$-V_S$
0	0	1	1	1	0	$-2V_S$
1	0	1	0	1	0	$-3V_S$

The above Table II is shows the active switches operation of seven level, 1 means the switch is ON, the 0 means the switch is OFF. Then we will get the seven level output voltage from the six switches only.

3.2Nine Level Multi Level Inverter (MLI)

Table- III
Nine level Multilevel (MLI)

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_0
0	1	0	1	1	0	1	0	$4V_S$
1	1	0	1	0	0	1	0	$3V_S$
0	0	0	1	1	1	1	0	$2V_S$
0	1	1	1	1	0	0	0	V_S
1	1	1	1	0	0	0	0	0
0	0	0	0	1	1	1	1	0
1	0	0	0	0	1	1	1	$-V_S$
1	1	1	0	0	0	0	1	$-2V_S$
0	0	1	0	1	1	0	1	$-3V_S$
1	0	1	0	0	1	0	1	$-4V_S$

The above Table III is shows the active switches operation of eight switches with nine level, 1 means the switch is ON, the 0 means the switch is OFF. Then we will get the nine level output voltage from the eight switches only.

3.3Eleven Level Multilevel inverter (MLI)

Table- IV
Eleven level multilevel Inverter (MLI)

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_0
0	1	0	1	1	0	1	0	$5V_S$
1	1	0	1	0	0	1	0	$4V_S$
0	1	0	0	1	0	1	1	$3V_S$
1	1	0	0	0	0	1	1	$2V_S$
0	1	1	1	1	0	0	0	V_S
1	1	1	1	0	0	0	0	0
0	0	0	0	1	1	1	1	0
1	0	0	0	0	1	1	1	$-V_S$
0	0	1	1	1	1	0	0	$-2V_S$
1	0	1	1	0	1	0	0	$-3V_S$
0	0	1	0	1	1	0	1	$-4V_S$
1	0	1	0	0	1	0	1	$-5V_S$

The above Table VI is shows the active switches operation of eight switches with eleven level, 1 means the switch is ON, the 0 means the switch is OFF. Then we will get the eleven level output voltage from the eight switches only.

3.4 Thirteen Level multi Level inverter

Table-V
Thirteen level multi level inverter (MLI)

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_0
0	1	0	1	1	0	1	0	$6V_S$
0	1	0	0	1	0	1	1	$5V_S$
1	1	0	1	0	0	1	0	$4V_S$
1	1	0	0	0	0	1	1	$3V_S$
0	1	1	1	1	0	0	0	$2V_S$
0	0	0	1	1	1	1	0	V_S
1	1	1	1	0	0	0	0	0
0	0	0	0	1	1	1	1	0
1	1	1	0	0	0	0	1	$-V_S$
1	0	0	0	0	1	1	1	$-2V_S$
0	0	1	1	1	1	0	0	$-3V_S$
0	0	1	0	1	1	0	1	$-4V_S$
1	0	1	1	0	1	0	0	$-5V_S$
1	0	1	0	0	1	0	1	$-6V_S$

The above Table V is shows the active switches operation of eight switches with thirteen level, 1 means the switch is ON, the 0 means the switch is OFF. Then we will get the thirteen level output voltage from the eight switches only.

3.5Different voltages are taken as the source voltages of the asymmetrical multilevel inverters

TABLE VI
DIFFEERENT VOLTAGES

No of levels	No of Switches	V1	V2	V3	Output Voltage in V
7	6	V_S	$2V_S$	-	$3V_S$
9	8	V_S	V_S	$2V_S$	$4V_S$
11	8	V_S	$2V_S$	$2V_S$	$5V_S$
13	8	V_S	$2V_S$	$3V_S$	$6V_S$

The seven level output voltage are get only from six switches only. The nine level, eleven level and thirteen level output voltage are get only from eight switches corresponding to respective voltage sources are taken.

The above table VI shows different voltages are taken for asymmetrical multilevel inverters. The asymmetrical multilevel inverters are simulated the output voltage are designed by using 200V. The seven level output voltage are get by using V1=66.66V, V2=133.33V. The nine level output voltage are get by using V1=50V, V2=50V, V3=100V. The eleven level output voltage are get by using V1=40V, V2=80V, V3=80V. The thirteen level output voltage are get by using V1=66.66V, V2=99.99V, V3=33.33V. The asymmetrical multilevel inverters are simulate the above written voltage values.

IV. MATLAB/SIMULATION RESULTS

4.1Basic circuit of Cascaded H-Bridge five level Inverter

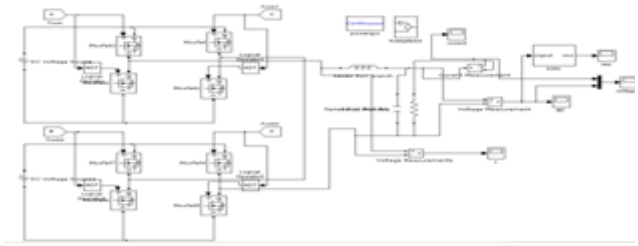


Fig.8 shows the five level inverter CHB simulink circuit

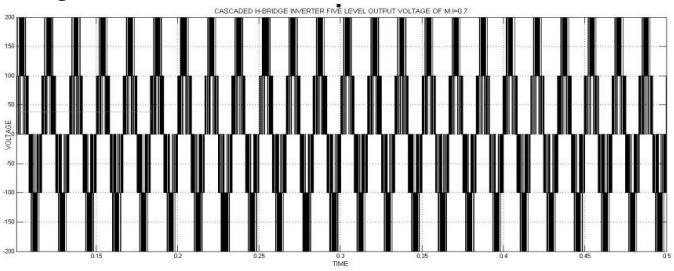


Fig.9 shows the five level output voltage CHB inverter without LC of M.I=0.7

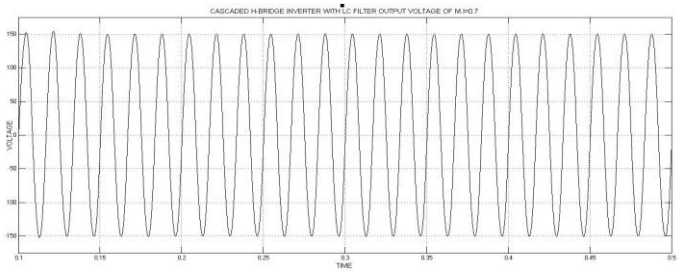


Fig.10 shows the output voltage with LC filter of CHB inverter of M.I=0.7

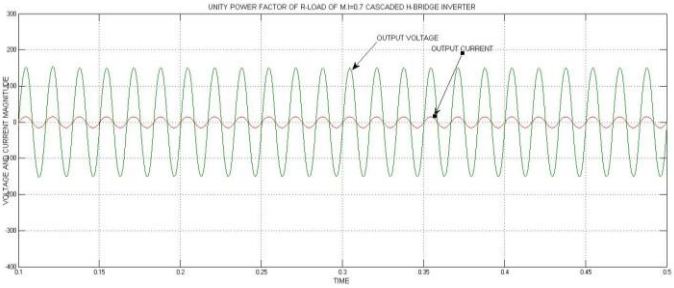


Fig.11shows the unity power factor at the R-Load with LC filter of CHB inverter of M.I=0.7

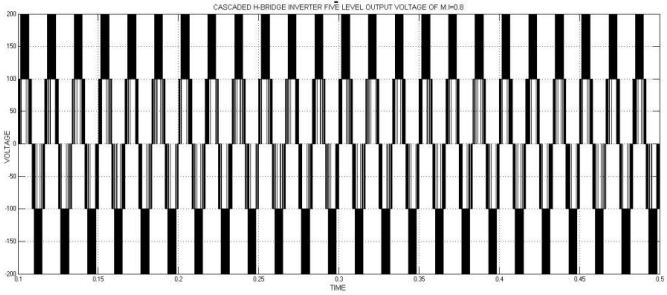


Fig.12 shows the five level output voltage CHB inverter without LC of M.I=0.8

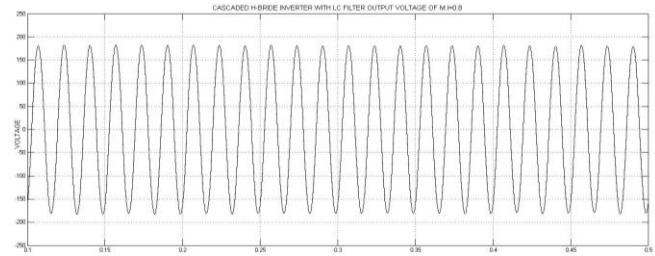


Fig.13 shows the output voltage with LC filter of CHB inverter of M.I=0.8

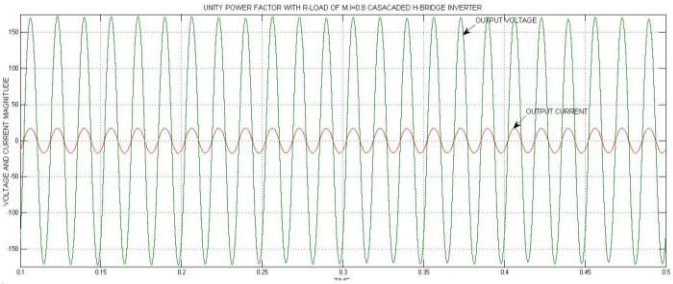


Fig.14 shows the unity power factor at the R-Load with LC filter of CHB inverter of M.I=0.8

Table-VII
Harmonics of CHB Inverter with and without LC

The Table VII shows the CHB inverter operating two modulation indexes. They are 0.7 and 0.8 without and with LC filter.

4.2 Simplified Five level Inverter

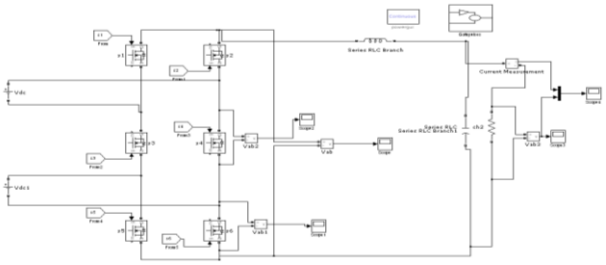


Fig.15. The simulink of simplified five level multilevel inverter

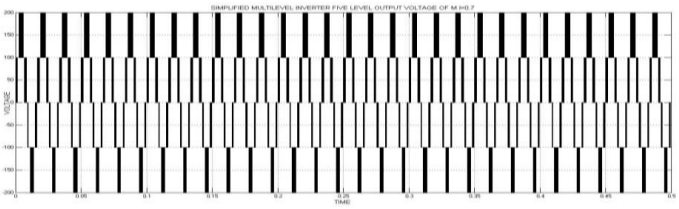


Fig.16 shows the five level output voltage of simplified five level inverter without LC of M.I=0.7

Harmonics	m_a =0.7	m_a =0.8
Fundamental 1	154.02	183.84
h3	2.40	3.31
h5	1.19	0.11
h7	0.24	0.07
h9	0.05	0.20
h11	0.02	0.09
%THD WITHOUT LC	0.146	0.114
%THD WITH LC	0.015	0.013

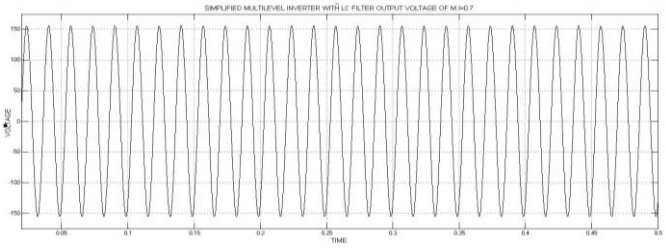


Fig.17 shows the output voltage with LC filter of simplified five level inverter of M.I=0.7

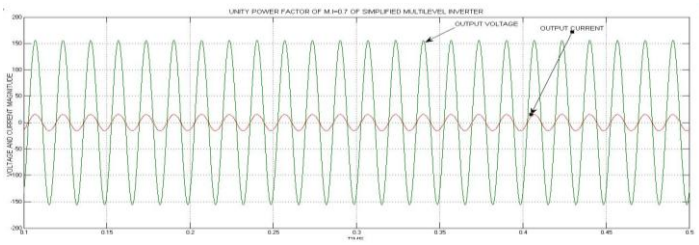


Fig.18 shows the unity power factor at the R-Load with LC filter of simplified five level inverter of M.I=0.7

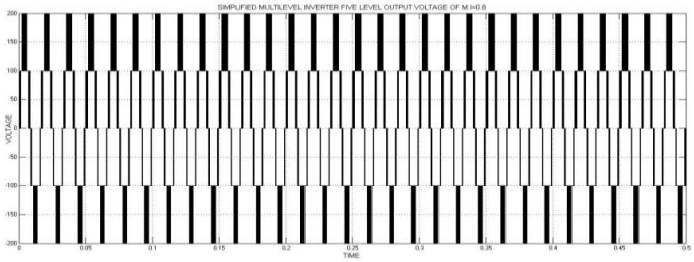


Fig.19 shows the five level output voltage simplified five level inverter without LC of M.I=0.8

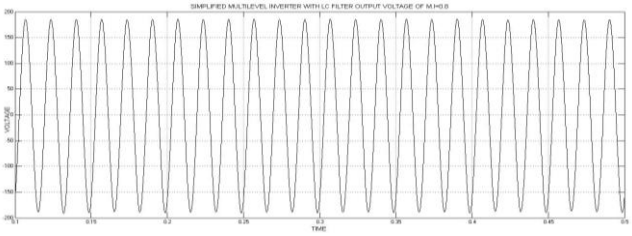


Fig.20 shows the output voltage with LC filter of simplified five level inverter of M.I=0.8

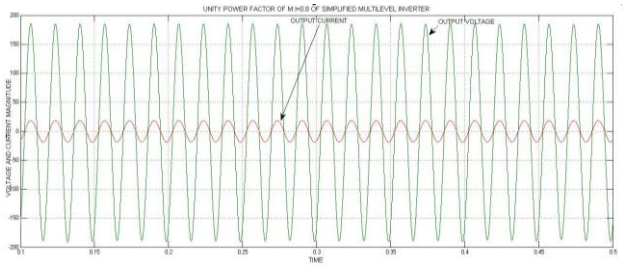


Fig.21 shows the unity power factor at the R-Load with LC filter simplified five level inverter of M.I=0.8

Table-VIII
Harmonics of Simplified Five Level Inverter with and without LC

Harmonics	m_a =0.7	m_a =0.8
Fundamental 1	157.77	185.66
h3	0.81	1.98
h5	0.25	0.17
h7	0.17	0.32
h9	0.06	0.06
h11	0.07	0.05
%THD WITHOUT LC	0.0701	0.0684
%THD WITH LC	0.005	0.003

The Table VIII shows the simplified five level inverter operating two modulation indexes. They are 0.7 and 0.8 without and with LC filter.

The modulating frequency (Switching frequency) is 18060Hz.

The CHB five level inverter operated with m_a =0.7 and m_a =0.8 with phase shift carrier pulse width modulation technique then I would get the fundamental component voltage increases and THD value decreases when modulation index m_a =0.8 compare to the m_a =0.7.The simplified five level inverter operated the same modulation index with phase disposition pulse width modulation technique then I would get the fundamental component voltage increases and THD value decreases compare to the CHB inverter. After clearly understand reduce the number of switches, improved output waveforms, smaller filter size and lower EMI of simplified multistring five level inverter compared to the CHB inverter.

4.3 Proposing system of Seven Level multilevel inverter

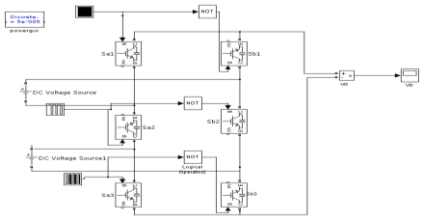


Fig.22 Simulink of the seven level multilevel inverter

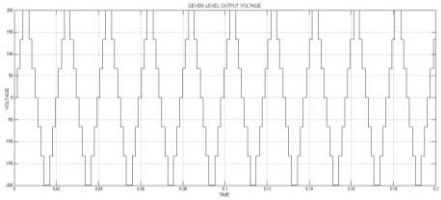


Fig.23 Seven level multivlevel Inverter output voltage

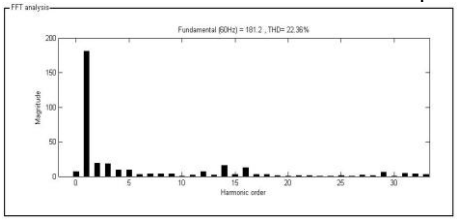


Fig.24THD value of the Seven level multilevel inverter using FFT analysis

4.4 Proposing System of Nine Level multilevel inverter

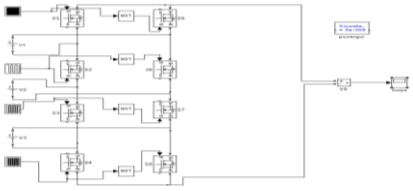


Fig.25 .Simulink of the nine, eleven and thirteen level multilevel inverter

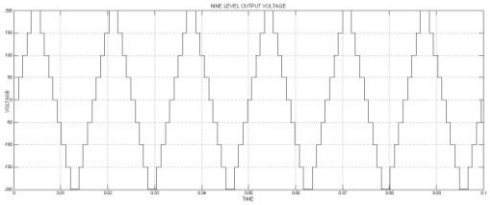


Fig.26 Nine level multilevel Inverter output voltage

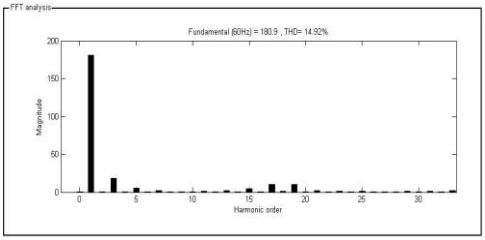


Fig.27 THD value of the nine level multilevel inverter using FFT analysis

4.4 Proposing System of Eleven Level multilevel inverter

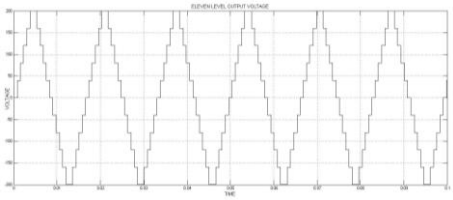


Fig.28 Eleven level mulitlevel Inverter output voltage

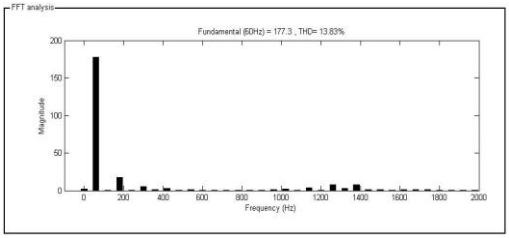


Fig. 29 THD value of the eleven level multilevel inverter using FFT analysis

4.5Proposing System of Thirteen Level multilevel inverter

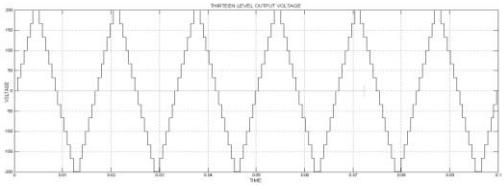


Fig.30 Thirteen level multilevel Inverter ouput voltage

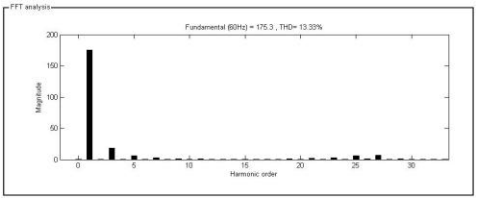


Fig.31 THD value of the thirteen level multilevel inverter using FFT analysis

Table-IX
Fundamental Component and THD value of the Multilevel inverter of Various Values

Magnitude of individual Harmonic content	No of Levels			
	7	9	11	13
Fundamental	181.25	180.90	177.34	175.34
h3	17.99	17.93	17.68	18.18
h5	9.11	5.21	5.43	5.79
h7	3.45	2.09	3.11	2.66
h9	3.71	0.05	1.23	1.21
h11	1.68	1.24	0.40	0.83
h13	2.32	2.19	0.79	0.07
h15	2.59	4.12	0.73	0.24
h17	2.81	10.16	2.08	0.79
h19	1.23	9.78	3.55	1.10
h21	0.86	2.17	7.70	1.69
h23	0.46	1.06	7.32	2.97
(%THD)	22.36 %	14.92%	13.83%	13.33%

Table-X
Dominant Harmonics in Various Multilevel inverters

Various Multilevel Inverter	Dominant Harmonics
Seven Level	$3^{rd}, 5^{th}, 9^{th}, 7^{th}$
Nine Level	$3^{rd}, 17^{th}, 19^{th}, 5^{th}$
Eleven Level	$3^{rd}, 21^{st}, 23^{rd}, 5^{th}, 19^{th}$
Thirteen Level	$3^{rd}, 5^{th}$

V. CONCLUSION

This work reports a Performance analysis of symmetrical and asymmetrical multilevel inverters, so reduce the number of switching devices, reduce the number of DC sources, driving circuits and cost reduces and also THD decreases.

Multistring multilevel inverters have low stress, high conversion efficiency and can also be easily interfaced with renewable energy sources (PV, Fuel cell). Asymmetrical multilevel inverter uses least number of devices to produce higher voltage level. As number of level increases, the THD content approaches to small value as expected. Thus it eliminates the need for filter. Though, THD decreases with increase in number of levels, some lower or higher harmonic contents remain dominant in each level. These will be more dangerous in induction drives.

Hence the future work may be focused to determine the pwm techniques of seven to thirteen level asymmetrical multilevel inverters.

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