

A Novel Soft Switching Lcl-T Buck Dc–Dc Converter System

A Mallikarjuna Prasad,¹ D Subbarayudu,² S Sivanagaraju³ U Chaithanya⁴

¹Research Scholar, JNTUK, Kakinada, A.P., India, 533003

²Director, Sreenivasa College of Engineering & Technology, Kurnool, India, 518004

³Associate Professor and HOD, JNTU Kakinada, Kakinada, India, 533003

⁴Assistant professor, ST.Johns College of Engineering & Technology, Kurnool, India, 518360

Abstract: The DC-DC Converter topologies have received increasing attention in recent years for Low power and high performance applications. The advantages DC-DC buck converters includes increased efficiency, reduced size, reduced EMI, faster transient response and improved reliability. The front end LCL-T in a buck converter is connected in sequence manner to improve the electrical performances and to reduce the switching losses. It futures several merits such as multi output capability and also will associate with one or two capacitors so has to improve resonant operations. This paper deals with simulation and implementation of LCL-T buck converter. Open loop and closed loop models are developed and they are simulated. The digital simulation is done by using MATLAB/SimPowerSystems tool and the simulation results are presented here.

Index Terms: Digital simulation, LCL-T buck converter, High input voltage.

I. Introduction

Generally a LC parameters buck converter topology and its variations exhibit satisfactory performance in majority of applications where output voltage is lesser than input voltage. The performance of buck converter can be improved by implementing a buck converter with multiple switches and/or extra inductor parameters.

With conventional method the four switches must withstand the input voltage during the ‘off’ period. In certain applications such as railway traction the input voltages values will be high. Then each transistor would sustain only half of input voltage. This approach beyond the safe operating point of power transistors. It has leded the designer with narrow applications. The best way to meet the requirements is to increase the breakdown voltage of a transistor. It leads to the disadvantages of higher on resistance and increases the cost then it would be better if the device is operated at half of the value of the voltage. In conventional method single transistor is assumed as two transistors connected in series. The two switches share the voltage equally, with voltage balancing components.

Then definitely the two transistors have to with stand only half of its input voltages. The conventional method approaches satisfy well with disadvantages of increase in cost of eight power switches for the circuit and the voltages balancing device. In this paper the two legs of a full bridge are connected in series. The node joining these two legs is held at half of the input voltage, using the bypass/filter capacitors which are connected two inputs of rails.

The proposed circuit can be operated with

- 1) Capacitive turn –off neglecting to reduce switching power losses during turn-off (snubbing).
- 2) Resonant changes over which leads to zero voltage turn-on so as to eliminate turn-on switching losses

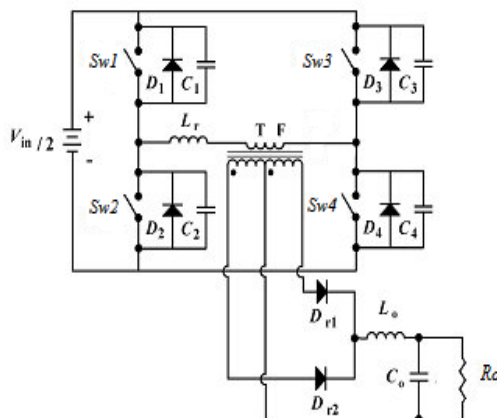


Fig 1. Conventional full-bridge converter

The coevals of new converter can be implemented by modifications in the connections of the components. First of all a capacitor is connected in series with a transformer as shown in fig 2.

The proposed converter circuit is designed by substituting input voltage source by two input capacitors as shown in fig 3. In this proposed circuit the upper leg consists of two switches Sw1 & Sw2 the lower leg consists of two switches Sw3 & Sw4.

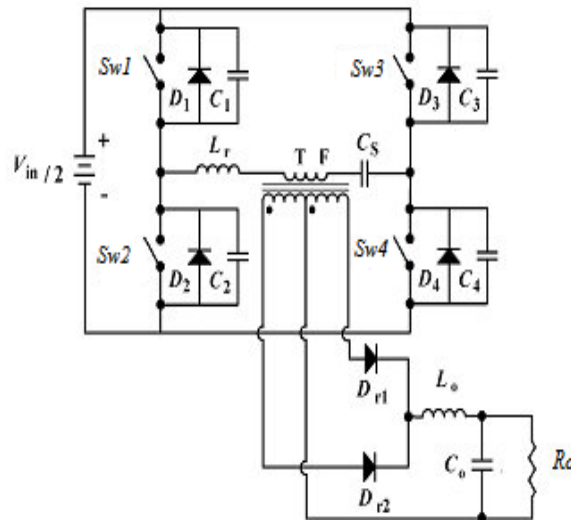


Fig. 2. Full-bridge converter with capacitor in series with transformer primary

II. LCL-T Buck Converter

The proposed converter is derived from the conventional full bridge topology presented in fig 1 and fig 2 respectively. Therefore, several operation characteristics of the full-bridge converter are also presented by the proposed structure. Fig 3 shows the power-stage circuit. The upper leg comprises The switches used in this circuit is metal oxide semiconductor field effect transistor (MOSFET). The internal substrate diode of a MOSFET switch conducts inverse polarity current and it also clamps the switching reverse voltage at about 1V, the capacitive turn-off snubbing is achieved by the MOSFET internal Con capacitances, which is used as C₁-C₄.

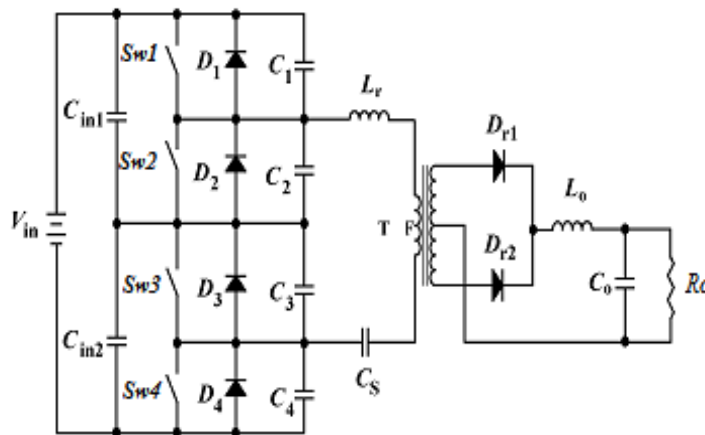


Fig.3. the proposed LCL-T Buck converter.

The capacitors Cin1 & Cin2 generate a bypassed dc midpoint voltage $V_{in}/2$ and by pass the input voltage.

When the switch is in "OFF" state each switch has a voltage of $V_{in}/2$ across its terminals. The dc voltage is blocked from being applied to L_r and TRF using the capacitance C_s the C_s capacitance value should be large enough to act as dc voltage source and to prevent the dc current being applied through L_r & TRF. The inductances L_r makes the capacitors C_1 - C_4 charges & discharges with its stored energy during the conduction period i.e provided between turning off one pair of switches & turning on the other pair. This makes the switch voltage to be zero before it is turned on. The isolation between the load and source is provided by the transformer. The diodes D_{r1} & D_{r2} rectify the rectangular wave output of a transformer. The inductances L_0 and capacitance C_0 filter the ripples from the rectified output.

From the output wave forms of proposed LCL-T type buck converter of fig 4, the voltage $V_{in}/2$ across the switches during off period is due to the join point of C_{in1} & C_{in2} which is at voltage $V_{in}/2$. The voltage across Sw1 or Sw2 is same as voltage at C_{in1} similarly the voltage of Sw3 or Sw4 are same as C_{in2} but both of those capacitor voltages are $V_{in}/2$.

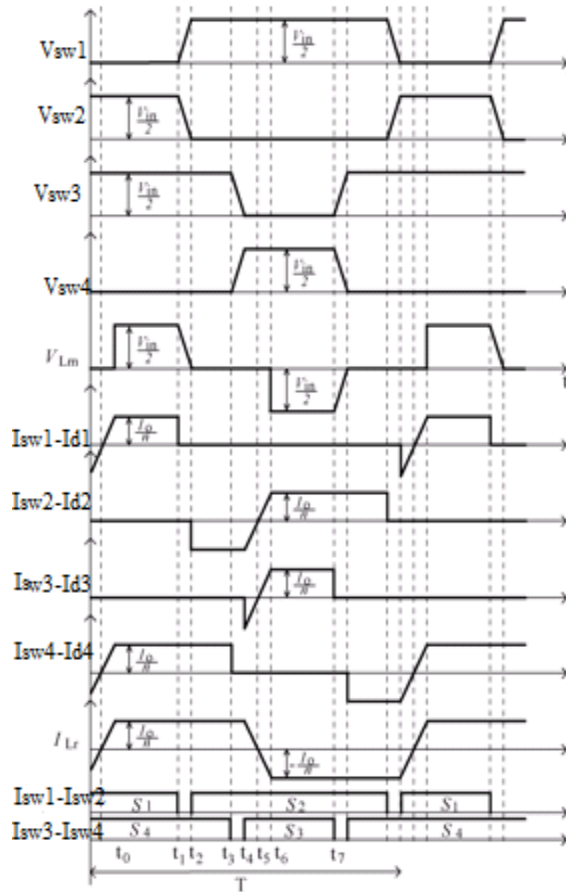


Fig.4. Waveforms of LCL-T type Buck Converter

The principle of operation is analyzed adopting ideal conditions, but some considerations must be done in a During the freewheeling period the capacitor's Cin1 & Cin2 will get charged & discharged, which occurs at the stage3 and at second half period of its operation .If the switch timing sequence of the switcher are a symmetry then the voltages across the capacitors can be other than the Vin/2. A very large asymmetry is needed to deviate from the ideal voltage value of Vin/2.

In first mode of operation the input capacitor's receiver energy from the source and in the sixth mode the stored energy is transferred to the load. The voltage source capacitor's are designed to have low ripple voltage 5% to 10%, these capacitor at converter start up discharged to Vcs=0. As server capacitance valve is very low. The voltage (Vcs) changes rapidly and in some switching cycle reaches a ideal valve. A current protection circuit is used to protect from excessive switch peak current during the transition.

B. Turn-On and Turn-Off Switching

Turn off:- In proposed converter the commutation process is similar to that of the classical Z Vs PWM full bridge converter. The loss that occurred during turned off are reduced by the snubber capacitors which are in parallel with the switches. The switch current flows through the commutation capacitor, changing the capacitor when it is turned off. Thus the capacitor voltage reaches the voltage Vc in. Due to this the voltage and current during crossing in the switch is minimized and the turn-off losses are minimized.

Turn on:- The proposed converter uses the zero-voltage turn-on to reduce the turn-on switching losses. The converter operating at high DC voltage the zero-voltage turn-on is very important, because the power dissipated in switching at non-zero discharged. Switches Sw2 and Sw4 turn-off in the power-transfer stage (stage 1 in Section III), and the output current referred to the primary accomplishes the charge and discharge of the snubber capacitors (linearly with time). The large stored energy of the ripple-filter inductor Lo is available for this purpose, so, as a practical matter, Sw2 and Sw4 and will always are turned-on at zero voltage.

But switches Sw3 and Sw4 turn-off in the free-wheeling stage during which the transformer is short circuited by the output rectifier. Thus, only the energy stored in the circuit inductance Lx (that includes the transformer primary- side leakage inductance) is available to charge and discharge the snubber capacitors, in a resonant way.

The minimum current that maintains zero-voltage turn-on for Sw1 or Sw3 is expressed in equation 1.

$$I_{min} = \frac{V_{in}}{2} \cdot \sqrt{\frac{2.C}{L_r}} \quad (1)$$

C is a snubber capacitor. The primary side current required to achieve zero-voltage turn on decreases as the value of (L_r) is large, but the inductance is limited by reduction of duty ratio.

III. SIMULATION RESULTS

Four switched Simulink model for LCL-T buck dc-dc converter is shown in fig 5, the input dc voltage is rectified into high switching AC frequencies using four switches LCL-T buck inverter.

Switching pulses are given to Sw1&Sw4, Sw2&Sw3 are shown in figures 6&7 and also their input voltages, output voltage & output current are shown in figures 8&9. The dc output voltage is variation at 600V.

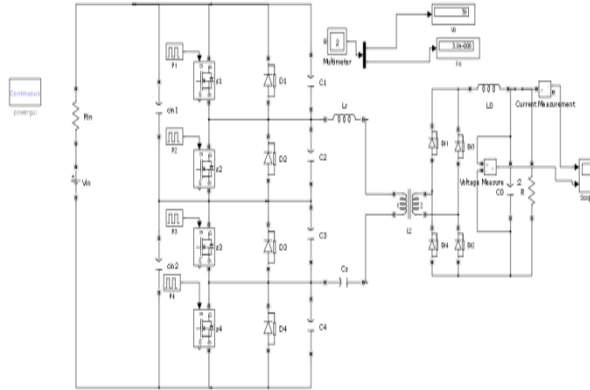


Fig 5. Simulation of the proposed LCL-T Buck converter.

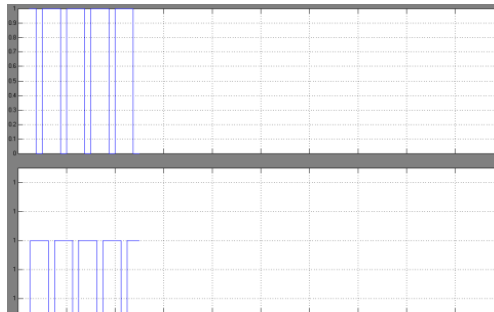


Fig 6. Driving pulses of S_1 & S_2

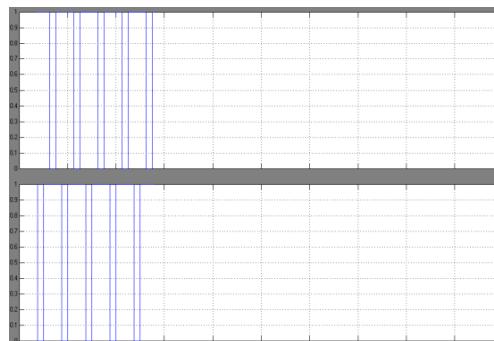


Fig 7. Driving pulses of S_3 & S_4

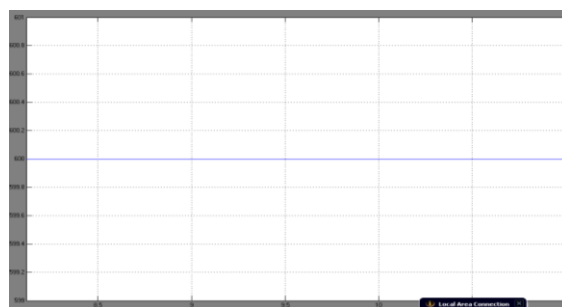


Fig.8 Input voltage

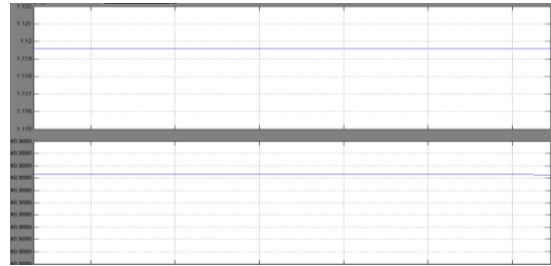


Fig.9 output voltage & output current

The closed loop system circuit model is shown in Fig 10. the closed loop system its output response is feedback and it is sensed, compared with an input reference voltage. The error can be through a PI controller. The output of PI controller refers with pulse width to maintain the output constant and their responses shown in Figures 11&12. it can be observe that the output voltage remains constant due to closed loop action of the system.

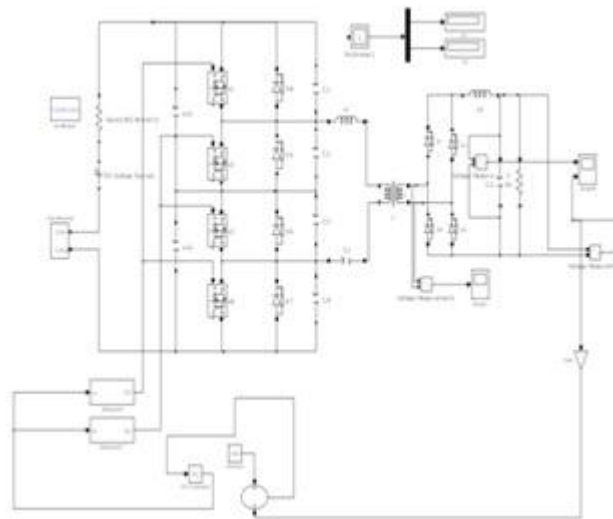


Fig.10. Closed loop model of two inductor boost Converter circuit

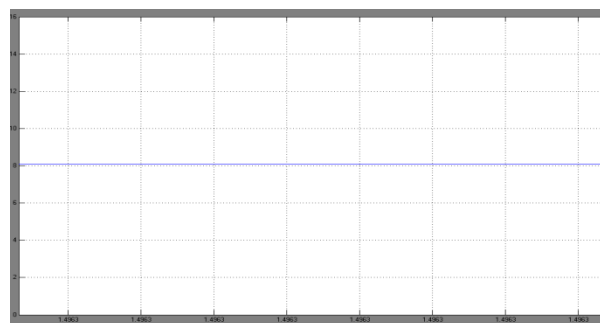


Fig.11 Input Voltage

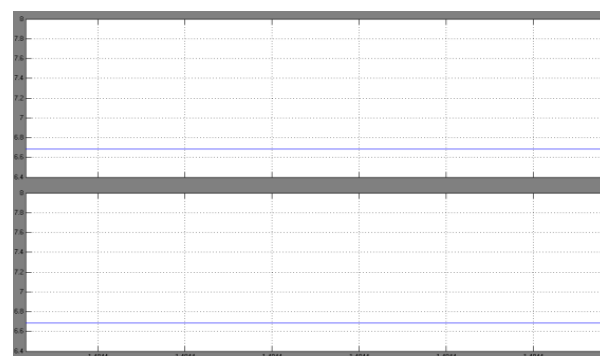


Fig.12. Output voltage with disturbance

IV. Conclusion

The proposed four switch LCL-T buck dc-dc converter system is simulated using MATLAB/Simulink and the results are presented. And it is observed the switching losses have been reduced and the converter output efficiency is more than that of conventional full bridge buck converter.

And the open loop & closed loop controlled four switched LCL-T buck dc-dc converter system is simulated using MATLAB/Simulink and the results are presented. The closed loop system acquires constant voltage. This four switch LCL-T power circuit topology is well suited to its economical-realization.

References

- [1] E. S. Kim, Y. B. Byun, T. G. Koo, K. Y. Joe, and Y. H. Kim, "An improved three level ZVZCS Dc/Dc converter using a tapped inductor and a snubber capacitor," in Proc. Power Conversion Conf. (PCC'02), Osaka, Japan, 2002, pp. 115–121.
- [2] E. S. Kim, Y. B. Byun, Y. H. Kim, and Y. G. Hong, "A three level ZVZCS phase-shifted Dc/Dc converter using a tapped inductor and a snubber capacitor," in Proc. IEEE Applied Power Electronics Conf. (APEC), 2001.
- [3] F. Canales, P. M. Barbosa, and F. Lee, "A zero voltage and zero current switching three-level dc/dc converter," in Proc. IEEE Applied Power Electronics Conf. (APEC), 2000, pp. 314–320.
- [4] T. F. Wu and J. C. Hung, "A PDM controlled series resonant multi-level converter applied for x-ray generators," in Proc. IEEE Power Electronics Specialists Conf. (PESC), 1999.
- [5] I. Barbi, R. Gules, R. Redl, and N. O. Sokal, "Dc/Dc converter for high input voltage: four switches with peak voltage of $V_{in}/2$, capacitive turn-off snubbing and zero-voltage turn-on," in Proc. IEEE Power Electronics Specialists Conf. (PESC), 1998, pp. 1–7.
- [6] R. Redl and L. Balogh, "Soft-switching full-bridge dc/dc converting," U.S. Patent 5 198 969, Mar. 30, 1993.
- [7] J. R. Pinheiro and I. Barbi, "The three-level ZVS-PWM DC-to-DC converter," IEEE Trans. Power Electron., vol. 8, pp. 486–492, Oct. 1993.
- [8] L. Balogh, R. Redl, and N. O. Sokal, "A novel soft-switching full-bridge DC-DC converter: analysis, design considerations, and experimental resultant 1.5 kW, 100 kHz," IEEE Trans. Power Electron., vol. 6, pp.408–418, July 1991.



A Mallikarjuna Prasad ,has graduated from MADRAS university in the year 2001 and obtained his M.E from Sathyabama University in the year 2004,his nine years of teaching experience ,exposed himself to be an authors for '3' titles currently he is working in the area of high power density dc-dc converters and also a research scholar in JNTU KAKINADA.



Dr D SubbaRayudu received B.E degree in Electrical Engineering from S.V. University, Tirupati, India in 1960; He has obtained his M.Sc (Engg) degree from Madras University in 1962 and Ph.D degree from Indian Institute of Technology, Madras, India in 1977. At present, he is working as Director in Sreenivasa College of engineering and Technology, Kurnool, India. Apart from his curriculum his interests is in Power Electronic Converters.



Dr S Sivanagaraju gained his Masters Degree in 2000 from IIT, Kharagpur and did his PhD from J.N.T. University in 2004. He is currently working as Associate professor and HOD in the Department of Electrical Engineering J.N.T.U. College of Engg, Kakinada, and Andhra Pradesh, India. For incredible performance he was awarded two national awards (*Pandit Madan Mohan Malaviya memorial prize award and Best paper prize award*) from the institution of engineers (India) for the year 2003-04. He is referee for IEE Proceedings-Generation Transmission and Distribution and also International journal of Emerging Electrical Power System. To his credit he has 50 publications in National and International journals and conference, His areas of interests Include, Distribution Automation, Genetic Algorithm application to distribution systems and Power Electronics.



U. CHAITHANYA has obtained his B.Tech from JNTU Ananthapur in the year 2008. He has obtained his M.Tech from JNTUUniversity Ananthapur in the year 2010. He has 3 years of teaching experience.. He is working in the area of high power electronics and control applications.