Indium Arsenide on Insulator Mosfets to Increase Carrier Mobility

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Abstract: *Silicon-on-insulator (SOI) MOSFET is one of the modern state of the art transistor in which a semiconductor layer like silicon is formed above an insulator layer on a semiconductor substrate. In SOI MOSFET, there is much more advantages over bulk silicon MOSFET such as high speed operation, low power consumption, small short channel effects. Over the past several years, the inherent scaling limitations of silicon (Si) electron devices have fuelled the exploration of alternative semiconductors, with high carrier mobility, to further enhance device performance. In particular, compound semiconductors heterogeneously integrated on Si substrates have been actively studied: such devices combine the high mobility of III–V semiconductors and the well established, low-cost processing of Si technology. This integration, however, presents significant challenges. Conventionally, heteroepitaxial growth of complex multilayer's on Si has been explored but besides complexity, high defect densities and junction leakage currents present limitations in this approach. Motivated by this challenge, we use a three surface potentials (gate oxide-silicon film interface, silicon-film-buried oxide interface and buried oxide-substrate interface) based compact model to study a fully depleted SOI and XOI MOSFETs. We have simulated the surface potentials, surface charge density, gate capacitance, drain current, transconductance and unity gain frequency of SOI and XOI MOSFETs. The different output characteristics show a better performance for InAs. We have got high drain current, transconductance and unity gain frequency of XOI MOSFET. On the other hand, we got very low (negative) threshold voltage for XOI MOSFET. So, by using XOI MOSFET, we can get high speed operation and amplification, low power consumption than SOI MOSFET as well as bulk silicon MOSFET.*

Keywords: *FD SOI MOSFET, In AS multilayter, Strong inversion, Poisson's equation, Surface potential based model, Transconductance*

I. INTRODUCTION

The SOI technology is introduced to overcome the limits of bulk or conventional Si MOSFETs. Among the problems are that the carrier mobility is decreasing due to impurity scattering, the gate tunneling current is increasing as the gate insulator becomes thinner, and the p-n junction leakage is increasing as the junction becomes shallower. These trends make the conventional scaling less and less feasible. As a result, the operating voltage is set higher than the expected value of a scaled-down device to achieve the desired speed performance and therefore the power dissipation goes high [2]. SOI CMOS offers a higher integration density than bulk CMOS. This high density results mainly from the absence of wells in SOI technology. SOI CMOS devices can be isolated by reach through oxidation, while bulk devices normally use junction isolation. SOI wafers can be processed in standard bulk silicon processing lines. As the feature size scaled down in modern IC technology, the source drain junction depth needs to be reduced to suppress short channel effects. In bulk silicon devices, such reduction may bring an unwanted interaction between the silicon and the metal such as metal punching through the junction. If the device is built on an SOI wafer, the source drain junction sits directly on dielectric layer (BOX) and no leakage occurs even the metal punches through the junction [3]. We considered epitaxial transfer method for the integration of ultrathin layers of single-crystal InAs on Si/ SiO2 substrates. As a parallel with silicon-on-insulator (SOI) technology14, we use 'XOI' to represent our compound semiconductor on-insulator platform.[12] Through experiments and simulation, the electrical properties of InAs XOI transistors are explored, elucidating the critical role of quantum confinement in the transport properties of ultrathin XOI layers. Importantly, a high-quality InAs/dielectric interface is obtained by the use of a novel thermally grown interfacial InAsOx layer (1 nm thick). The fabricated field-effect transistors exhibit a peak transconductance of 1.6mSmm21 at a drain–source voltage of 0.5 V, with an on/off current ratio of greater than 10,000.

II. ADOPTED TECHNIQUE

The main objective of our work is performance comparison between InAs-on-Insulator and Silicon-on-Insulator MOSFETs using a compact model. First of all, we follow a model as discussed in Ref. [9] which uses three surface potentials. However, before proceed to our objective, we want to verify our model with the results of Ref. [9]. After verifying the model, we want to change the channel material to InAs by replacing Si and then to compare the performance. For fair comparison the device dimensions, doping densities will be assumed same. Then after calculating surface potential, using this we want to compare the C-V characteristics and the drain current. From the I_D-V_{GS} curve, we can calculate the threshold voltage, on and off current ratio of the MOSFET. Then we also want to observe the difference between transconductance and unity gain frequency of InAs-on-Insulator and Silicon-on-Insulator MOSFET.

III. MODEL

3.1 Ideal Surface Potential Model

To obtain a closed-form analytical approximation for potentials at the three surfaces of the FDSOI MOSFET, namely front oxide–silicon film surface φ_{sf}, buried oxide–silicon film interface φ_{sb}, and buried oxide–substrate interface φ_{sbulk}. For this purpose, three different equations are obtained by solving the 1-D Poisson equation in vertical direction and applying the boundary conditions at different surfaces [9]. The 1-D Poisson equation of an FD-SOI MOSFET, shown in Figure 2-1, can be written as:

$$\frac{\partial^2 \varphi(y)}{\partial y^2} = -\frac{1}{\varepsilon_{Si}}\left(p(y) - n(y) - N_{ch}\right) \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (1)$$

Where $\varphi(y)$ is the potential, ε_{Si} is the dielectric constant of silicon, $p(y)$ and $n(y)$ are the hole and electron concentrations, respectively and N_{ch} is the doping in the silicon layer [9].
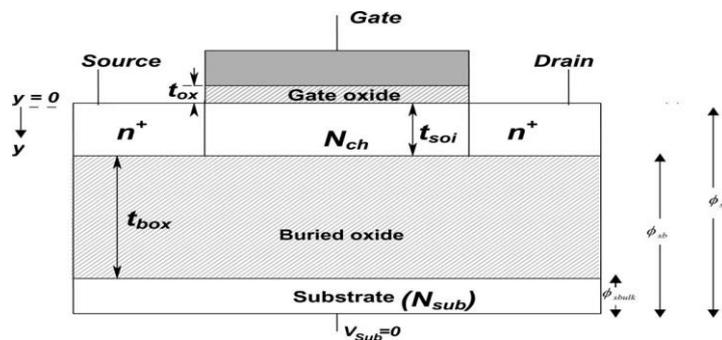

Fig .1. Cross-sectional view of the FD SOI MOSFET [9]

Equation (1) can be further expressed as

$$\frac{\partial^2 \varphi(y)}{\partial y^2} = -\frac{qN_{ch}}{\varepsilon_{Si}}\left\{\left[\exp\left(-\frac{\varphi(y)}{\varphi_t}\right) - 1\right] - \exp\left(-\frac{2\varphi_F + V_{CB}}{\varphi_t}\right)\left[\exp\left(\frac{\varphi(y)}{\varphi_t}\right) - 1\right]\right\} \cdots (2)$$

Where φ_F is the Fermi potential, φ_t is the thermal voltage, and V_{CB} is the channel floating body potential, which varies from V_{SB} at source to $V_{SB} + V_{DS}$ at drain [9]. Multiplying both sides of Eq. (2) by $2\dfrac{\partial\varphi(y)}{\partial y}$ and then integrating from buried oxide–silicon film interface φ_{sb} to front oxide–silicon film surface φ_{sf} considering boundary conditions we get,

$$\left(V_g - \varphi_{sf}\right)^2 - \frac{C_{box}^2}{C_{ox}^2}\left(\varphi_{sbulk} - \varphi_{sb}\right)^2 = -\gamma^2\left\{\begin{array}{l}-\varphi_t\left[\exp\left(-\frac{\varphi_{sf}}{\varphi_t}\right) - \exp\left(-\frac{\varphi_{sb}}{\varphi_t}\right)\right]\\ -\left(\varphi_{sf} - \varphi_{sb}\right) - \exp\left(-\frac{2\varphi_F + V_{CB}}{\varphi_t}\right)\\ \left(\varphi_t\left[\exp\left(\frac{\varphi_{sf}}{\varphi_t}\right) - \exp\left(\frac{\varphi_{sb}}{\varphi_t}\right)\right] - \left(\varphi_{sf} - \varphi_{sb}\right)\right)\end{array}\right\}$$

$$\cdots\cdots\cdots\cdots (3)$$

$$\varphi_{sf} - \varphi_{sb} = \alpha + \left(\varphi_{sb} - \varphi_{sbulk}\right)\frac{C_{box}}{C_{soi}} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (4)$$

$$\varphi_{sb} = \varphi_{sbulk} + \gamma_{bulk} \sqrt{\varphi_{sbulk}} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (5)$$

Where, $\gamma_{bulk} = \dfrac{\sqrt{2qN_{sb}\varepsilon_{Si}}}{C_{box}}$, $\alpha = \dfrac{qN_{ch}t_{soi}^2}{2\varepsilon_{Si}}$, $C_{soi} = \dfrac{\varepsilon_{ox}}{t_{soi}}$ and $C_{box} = \dfrac{\varepsilon_{ox}}{t_{box}}$.

Equations (3), (4) and (5) together describe the exact Poisson equation for an FDSOI MOSFET and are obtained without any approximation except the assumptions that the back silicon surface and the substrate region never go into inversion and that the device always remains in FD condition. These equations can be solved iteratively to get the exact values of all three surface potentials [9].

3.2 Drain Current Model
The surface potential nor the depletion charge density changes much after strong inversion. The central assumption of the charge-sheet model for the depletion charge density,

$$Q_d = -qN_aW_d = -\sqrt{2\varepsilon_{Si}qN_a\varphi_{sf}} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (6)$$

Can be extended to beyond strong inversion. Since the total silicon charge density Q_s is given by

$$V_{GS} = V_{FB} + \varphi_{sf} - \dfrac{Q_s}{C_{ox}} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (7)$$

Now Eq. (6) allows the inversion charge density to be expressed as

$$Q_i = Q_s - Q_d = -C_{ox}\left(V_{GS} - V_{FB} - \varphi_{sf}\right) + \sqrt{2\varepsilon_{Si}qN_a\varphi_{sf}} \quad \dots\dots\dots\dots\dots (8)$$

It should be noted that the charge sheet model does not literally assume all the inversion charge is located at the silicon surface with a zero depth.

The variable in the drain current integral, $I_{ds} = \mu_{eff} \dfrac{W}{L} \int_0^{V_{DS}} (-Q_i(V))dV \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (9)$

Can be transformed from V to φ_{sf}, $I_{ds} = \mu_{eff} \dfrac{W}{L} \int_{\varphi_{ss}}^{\varphi_{sd}} \left(-Q_i\left(\varphi_{sf}\right)\right)\dfrac{dV}{d\varphi_{sf}}d\varphi_{sf} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (10)$

Where φ_{ss}, φ_{sd} are the values of the surface potential at the source and the drain ends of the channel

3.3 Surface Electric Field and Surface Charge

Conventionally, the electrostatic potential is defined in terms of the intrinsic Fermi level,

$$\varphi_i = -\dfrac{E_i}{q} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (11)$$

There is a negative sign because E_i is defined as electron energy while φ_i is defined for a positive charge. The electric field E_s which is defined as the electrostatic force per unit charge is to the negative gradient of φ.

$$E_s = -\dfrac{d\varphi}{dy} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (12)$$

Now we can write Poisson's equation as $\dfrac{d^2\varphi}{dy^2} = -\dfrac{dE_s}{dy} = -\dfrac{\rho_{net}(y)}{\varepsilon_{Si}}$ .... (13)

Where $\rho_{net}(y)$ is the net charge density per unit volume at y, and ε_{Si} is the permittivity of silicon equal to $11.7\varepsilon_0$. Here $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm is the vacuum permittivity [11].

Another form of Poisson's equation is Gauss's law, which is obtained by integrating Eq. (13)

$$E_s = \frac{1}{\varepsilon_{Si}} \int \rho_{net}(y)dy = \frac{Q_s}{\varepsilon_{Si}}$$ .... (14)

Where Q_s is the integrated charge density per unit area. Now the surface charge can be obtain from Eq. (7) if φ_{sf} is known

$$Q_S = -C_{ox}(V_{GS} - V_{FB} - \varphi_{sf})$$ .... (15)

Therefore the surface electric field becomes [11]

$$E_S = -\frac{C_{ox}}{\varepsilon_{Si}}(V_{GS} - V_{FB} - \varphi_{sf})$$ .... (16)

3.4 Capacitances of MOS Structure

We now consider the capacitances of a MOS structure. In most cases, MOS capacitances are defined as small-signal differential of charge with respect to voltage or potential. The total MOS capacitance per unit area is [11]

$$C_g = \frac{d(-Q_s)}{dV_g}$$ .... (31)

By substituting the value of Q_s, we get

$$C_g = C_{ox}\left\{\frac{\rho(\varphi_{sf})^{\frac{1}{2}}}{\rho(\varphi_{sf})^{\frac{1}{2}} + k_0\dfrac{q}{kT}\left(1 + \dfrac{n_i^2}{N_A^2}e^{\frac{q\varphi_{sf}}{kT}}\right)}\right\}$$ .... (32)

Where $$\rho(\varphi_{sf}) = \frac{q}{kT}\varphi_{sf} + \frac{n_i^2}{N_A^2}e^{\frac{q\varphi_{sf}}{kT}}$$

IV. PERFORMANCE IMPROVEMENT FOR XOI MOSFET WITH RESPECT TO SOI

The three surface potential based compact model is used to generate the surface potentials and then the front surface potential is used to calculate the I-V and C-V curves for performance comparison between the SOI and XOI MOSFETs. The different parameters used for the InAs XOI MOSFET are shown in Table 1. These parameters have been used in Ref. [12]. For fair comparison, the same device dimensions and doping densities are assumed for the SOI MOSFET.
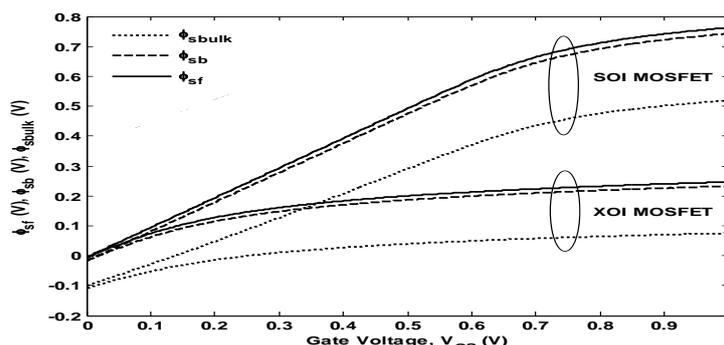

Figure. 2. Different surface potentials versus gate voltage curve

Figure 1-2 shows the variation of surface potentials φ_{sf}, φ_{sb} and φ_{sbulk} versus the gate voltage of SOI and XOI MOSFETs for a front oxide thickness of 7 nm, buried oxide thickness of 50 nm and silicon film thickness of 15 nm. Here, the surface potential curves of XOI MOSFET are saturated quicker than SOI MOSFET. We have got small saturation value of front surface potential because a large potential drops across the gate oxide and a smaller voltage drops across the channel thickness of XOI MOSFET.

Table 1: Simulation parameters of SOI and XOI MOSFETs [12]

Subject	SOI	XOI
Flat Band voltage, V_{fb}	-0.2 V	-0.2V
Electron concentration in channel, N_{ch}	4×10^{16} cm^{-3}	4×10^{16} cm^{-3}
Electron concentration in substrate, N_{sub}	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}
Intrinsic concentration, η_i	1.5×10^{10} cm^{-3}	1×10^{15} cm^{-3}
Gate Oxide thickness, t_{ox}	7 nm	7 nm
Buried Oxide thickness, t_{box}	50 nm	50 nm
Channel Thickness, t_{soi}	15 nm	15 nm
Vacuum Permittivity, ε_o	8.854×10^{-12} F/m	8.854×10^{-12} F/m
Relative permittivity of silicon dioxide, $\varepsilon_{t,ox}$	3.9	3.9
Relative permittivity of Zirconium dioxide, ε_t	20	20
Electron mobility, μ_e	650 cm^2/V-s	1300 cm^2/V-s
Channel Length, L	500 nm	500 nm
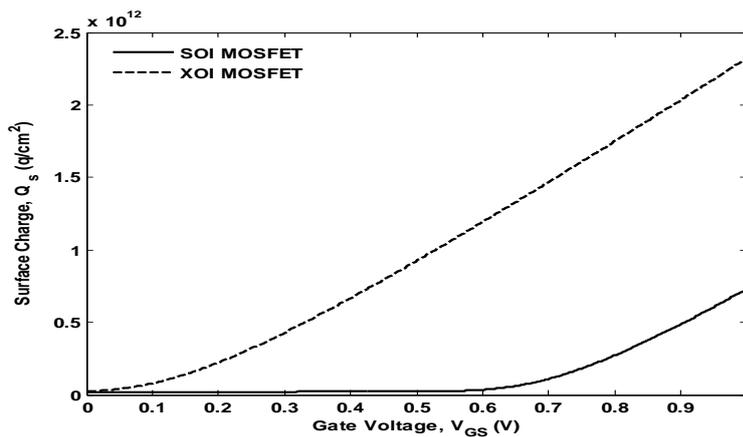
Figure. IV. Surface charge versus gate voltage curve

Figure 1-3 shows the surface charge density versus gate voltage curve between SOI and XOI MOSFETs. There are two regions of the curve. The flattened region represents the weak inversion region and the rising part is the strong inversion region. Since the inversion charge density increases rapidly with an increase in gate voltage as we have seen in the Figure 3-4. It occurs like that the surface potential changes with gate voltage and the electron concentration increases rapidly with very small changes in surface potential. We have observed, for XOI MOSFET the surface charge curve reaches in strong inversion region earlier than SOI MOSFET. For this, the surface potentials of XOI MOSFET saturated earlier than SOI MOSFET.
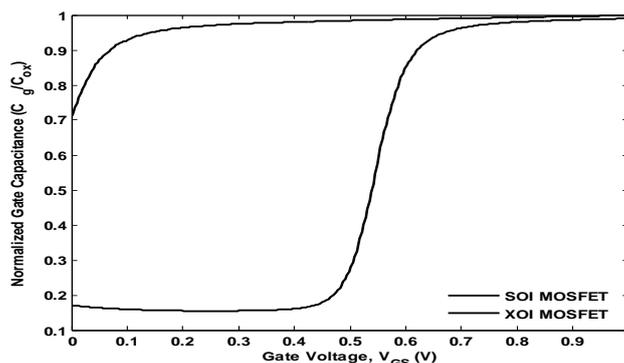
Figure.4. Gate capacitance versus gate voltage curve

For SOI MOSFET at first the curve is flat and the capacitance value is small because the FET turns on at $V_{GS} \approx$ 0.45 V. After the FET is turned on, the capacitance rapidly increases with gate bias and saturates to C_{ox} at strong inversion. The gate capacitance of the XOI FET quickly saturates to C_{ox} because the XOI FET turns on at a very small gate bias.
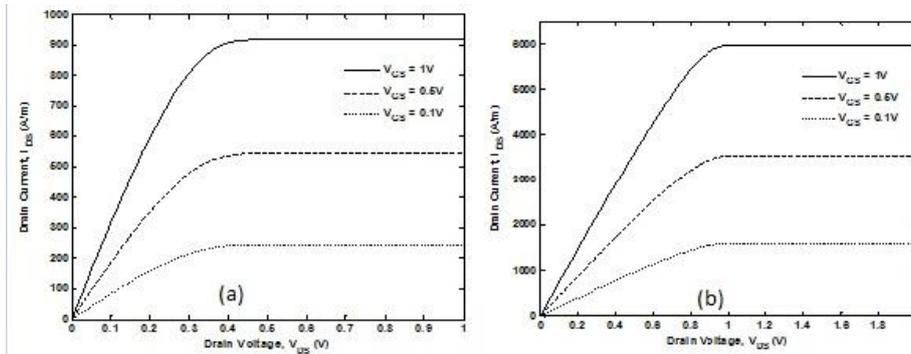

Figure. 1. $I_D - V_{DS}$ **Characteristics curves of SOI and XOI MOSFETs**

Figure 1-5(a) and (b) show $I_D - V_{DS}$ characteristics curves of SOI and XOI MOSFETs respectively for different gate voltages. When V_{GS} changes, the I_D versus V_{DS} curve will change. We saw that, if V_{GS} increases, the initial slope of I_D versus V_{DS} increases. The drain current in saturation is virtually independent of V_{DS} and the MOSFET acts as a current source.
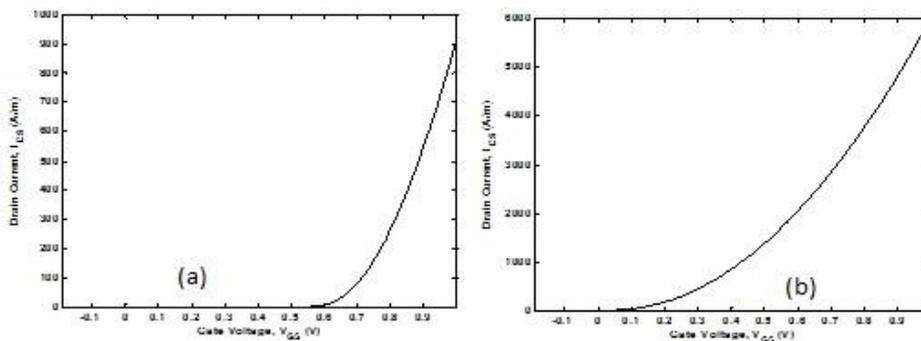

Figure. 6. Gate capacitance versus gate voltage curve
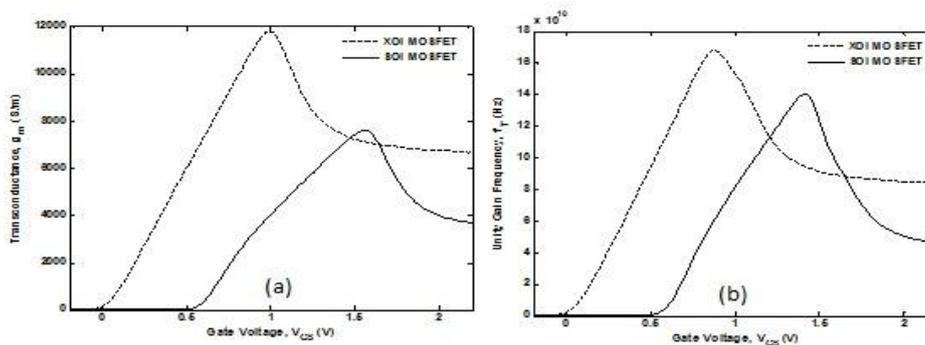

Figure.7. Gate capacitance versus gate voltage curve

Figure 1-6 shows the transconductance versus gate voltage characteristics curve for SOI and XOI MOSFETs for V_{DS} = 0.5 V and L = 500 nm. The MOSFET transconductance is defined as the change in drain current with respect to the corresponding change in gate voltage. The transconductance increase linearly with V_{DS} but is independent of V_{GS} in the saturation region. The transconductance is also a function of the geometry of the device as well as of carrier mobility and threshold voltage. For XOI MOSFET, transconductance is around 1.2 times higher than that of SOI MOSFET. This is because the carrier mobility of InAs is higher than that of Si.

Figure 1-7 shows the unity gain frequency versus gate voltage characteristics curve of XOI and SOI MOSFETs. The unity gain frequency of a MOSFET (f_T) is defined as the frequency at which the short-circuit current-gain (i_d / i_g) of the common-source amplifier becomes unity. f_T is also called the transition frequency. f_T gives an idea of the high-frequency behavior of the MOSFET. In XOI MOSFET, unity gain frequency f_T is 1.2 times higher than SOI MOSFET. Higher f_T means higher transconductance and lower internal MOSFET capacitances which means better amplification. So, by using XOI MOSFET, we can amplify signal more than SOI MOSFET.

V. CONCLUSION

From the simulation results, we observe that, for the same device dimensions and doping densities of the SOI and XOI MOSFETs, we got around 6 times higher drive current, around 1.5 times higher transconductance and around 1.2 times higher unity gain frequency. On the other hand, we got very low (negative) threshold voltage for XOI MOSFET. After the analysis, we see that, to overcome the limitations of bulk silicon MOSFET, we can use SOI MOSFET which can be solved the scaling problems. And over SOI MOSFET, XOI MOSFET has better performance because of high carrier mobility of compound semiconductors such as III-V semiconductors. So, by using XOI MOSFET, we can get high speed operation and amplification, low power consumption than SOI MOSFET as well as bulk silicon MOSFET.

REFERENCES

[1]   Narayana Murty Kodeti, "White paper on Silicon-on-insulator (SOI) implementation", Infotech Enterprises Ltd., pp. 3-8, June 2009
[2]   Takayasu Sakurai, Akira Matsuzawa, and Takakuni Douseki, "Fully depleted SOI CMOS circuits and technology for ultra-low power applications", First edition, Springer, ch. 1, pp. 1-19, 2006
[3]   John Z. Ren, "Low voltage SOI MOSFET with suppressed floating body effects", Master of Applied Science thesis paper, University of Toronto, pp. 9-17, 1999
[4]   Aatish Kumar, V. Ramgopal Rao and Prof. Rakesh Lal, "Simulation and characterization of SOI MOSFETs", Dual degree project report, Indian Institute of Technology, Mumbai, pp. 49-50, 2001
[5]   http://en.wikipedia.org/wiki/SiliconOnInsulator
[6]   Zhou Xing, Lim Khee Yong, "A general approach to compact threshold voltage formulation based on 2D numerical simulation and experimental correlation for deep submicron ULSI technology development", IEEE Transactions on Electron Devices, vol. 47, pp. 214-221, January 2000
[7]   Neil H. E. Weste, Kamran Eshraghian, "Principles of CMOS VLSI Design", Second edition, Addison Wesley, ch. 2, pp. 27-35, October 1994
[8]   Haldun Haznedar, "Digital Microelectronics", First edition, Benjamin-Cummings publication company, ch. 5, pp. 174-181, January 1991
[9]   Pradeep Agarwal, Govind Saraswat, and M. Jagadesh Kumar, "Compact surface potential model for FD SOI MOSFET considering substrate depletion region", IEEE Transactions on Electron Devices, vol. 55, no. 3, pp. 789-795, March 2008
[10]   J. R. Brews, "A charge-sheet model of the MOSFET," Solid State Electron., vol. 21, pp. 345-346, 1978
[11]   Yuan Taur, Tak H. Ning, "Fundamentals of modern VLSI devices," Second edition, Cambridge University Press, ch. 2-3, pp. 52-90, 2009
[12]   Hyunhyub Ko, Kuniharu Takei, Rehan Kapadia, Steven Cguang, Hui Fang, Paul W. Leu, Kartik Ganapathi, Elena Plis, Ha Sul Kim, Szu-Ying Cgen, Morten Madsen, Alexandra C. Ford, Yu-Lun Chueh, Sanjay Krishna, Sayeef Salahuddin & Ali Javey, " Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors", Nature, vol. 468, pp. 286-289, November, 2010
[13]   Takayasu Sakurai, Akira Matsuzawa, and Takakuni Douseki, "Fully depleted SOI CMOS circuits and technology for ultra-low power applications", First edition, Springer, ch. 8, pp. 372-373, 2006
[14]   Dieter K. Schrodera and Jeff A. Babcock, "Negative bias temperature instability: road to cross in deep submicron silicon semiconductor manufacturing", Applied Physics Reviews- Focus Review, pp. 5-6, July 2003