Simulink Modeling of Novel Hybrid H-Bridge Inverter for Smart Grid Application

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Abstract: *Hybrid H- bridge inverter. The proposed novel cascaded Hybrid H-bridge produces higher voltage levels with less number this paper presents a single-phase multistring Multi-level photovoltaic (PV) inverter topology for Micro grid-connected PV systems with a novel of devices. This will reduce the number of gate drives and protection circuits requirement, this inurn reduces the cost increase the reliability. Design Procedure for various components of single Hybrid H- bridge cell is given. A cascaded Grid connected PV topology is proposed. Finally a Matlab/Simulink based model is developed and simulation results are presented.*

Keywords:*PVCell, Hybridge H-bridge, Multi-lebel phovoltaic(PV) inverter, Matalab/Simulink, Micro grid-connected PV System;*

I. Introduction

Natural quantity available, it has been spotlighted as the future energy sources of promising potentiality, due As the PV system is clean and large enough in the to the stable supply of the energy and alternative method of responding to the problem of the earth environment followed by the increase of the demand for the electric power supply. Solar-electric-energy demand has grown consistently by 20%–25% per annum over the past 20 years, which is mainly due to the decreasing costs and prices. This decline has been driven by the following: 1) an increasing efficiency of solar cells; 2) manufacturing-technology improvements; and 3) economies of scale [2]. A PV inverter, which is an important element in the PV system, is used to convert dc power from the solar modules into ac power to be fed into the grid. A general overview of different types of PV inverters is given in [3] and [4].

In recent years, multilevel converters have shown some significant advantages over traditional two-level converters, especially for high power and high voltage applications. In addition to their superior output voltage quality, they can also reduce voltage stress across switching devices. Since the output voltages have multiple levels, lower d*v/dt is achieved, which greatly alleviates electromagnetic* interference problems due to high frequency switching. Over the years most research work has focused on converters with three to five voltage levels, although topologies with very high number of voltage levels were also proposed. In general, the more voltage levels a converter has the less harmonic and better power quality it provides. However, the increase in converter complexity and number of switching devices is a major concern for multilevel converter. There are several topologies available, being the Neutral Point Clamped [5], Flying Capacitor [6] and Cascaded H bridge inverter [7] the most studied and used. In recent years many variations and combinations of these topologies have been reported, one of them is the cascaded H-bridge [7-10].

II. High Power Converters Classifications

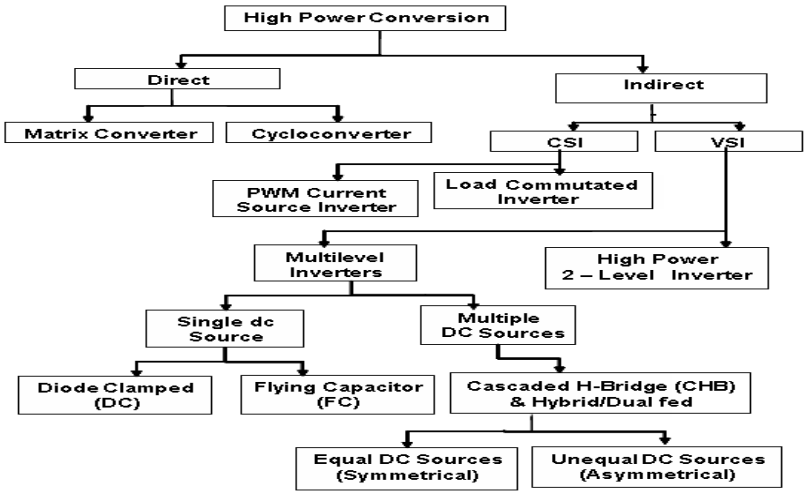

Figure 1 Classification of High power Converters

Fig.1 shows the classification of high power converters. Out of all converters Cascaded bridge configuration is more popular. Cascaded bridge configuration is again classified into 2 types 1) Cascaded Half Bridge 2) Cascaded Full Bridge or Cascaded H-Bridge. In this paper a novel cascaded hybrid H- Bridge topology is proposed for PV application.

A Half H-Bridge

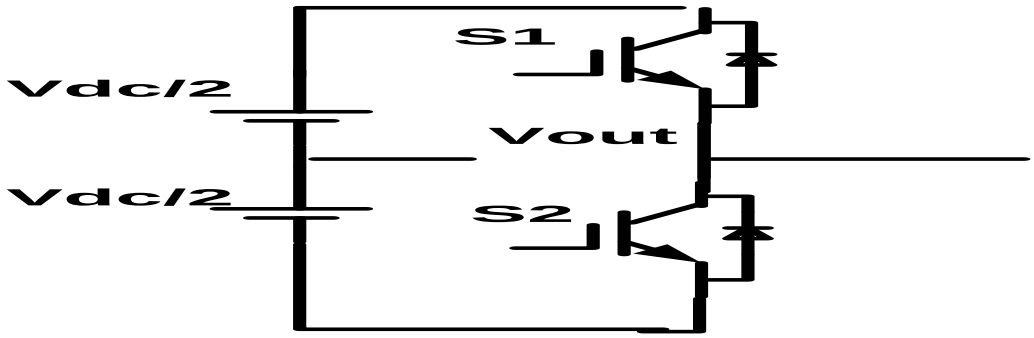

Figure 2 Half Bridge

Fig.2 shows the Half H-Bridge Configuration. By using single Half H-Bridge we can get 2 voltage levels. The switching table is given in Table 1

Table 1. Switching table for Half Bridge

Switches Turn ON	Voltage Level
S2	Vdc/2
S1	-Vdc/2

B Full H-Bridge

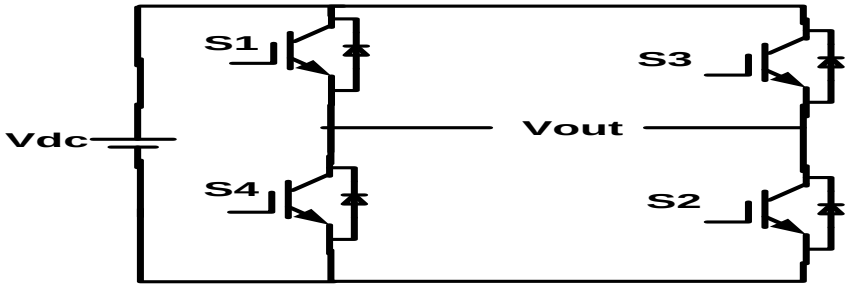

Figure. 3 Full H-Bridges

Fig.3 shows the Full H-Bridge Configuration. By using single H-Bridge we can get 3 voltage levels. The number output voltage levels of cascaded Full H-Bridge are given by 2n+1 and voltage step of each level is given by Vdc/n. Where n is number of H-bridges connected in cascaded. The switching table is given in Table2

C Hybrid H-Bridge

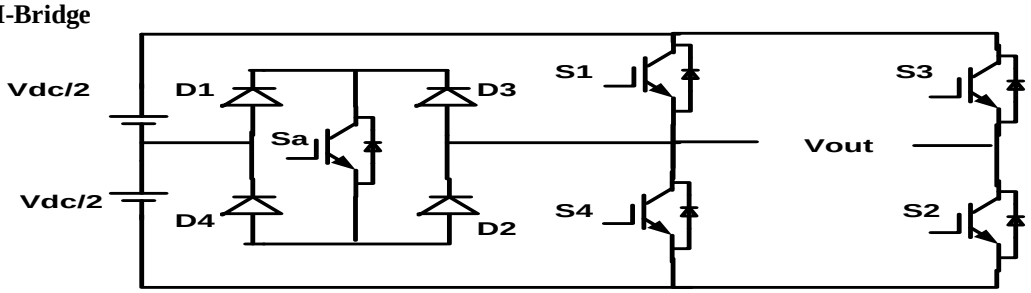

Table 2. Switching tabe Full Bridge

Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

Figure. 4 Hybrid H-Bridges

Fig. 4 shows the Hybrid H-Bridge configuration. By using single Hybrid H-Bridge we can get 5 voltage levels. The number output voltage levels of cascaded Hybrid H-Bridge are given by 4n+1 and voltage step of each level is given by Vdc/2n. Where n is number of H-bridges connected in cascaded. The switching table of Hybrid H-Bridge is given in Table 3.

Table 3. Switching table for Hybrid H-Bridge

Switches Turn On	Voltage Level
Sa, S2	Vdc/2
S1,S2	Vdc
S4,D2	0
Sa,S3	-Vdc/2
S3,S4	-Vdc

D Cascaded Hybrid H-Bridge

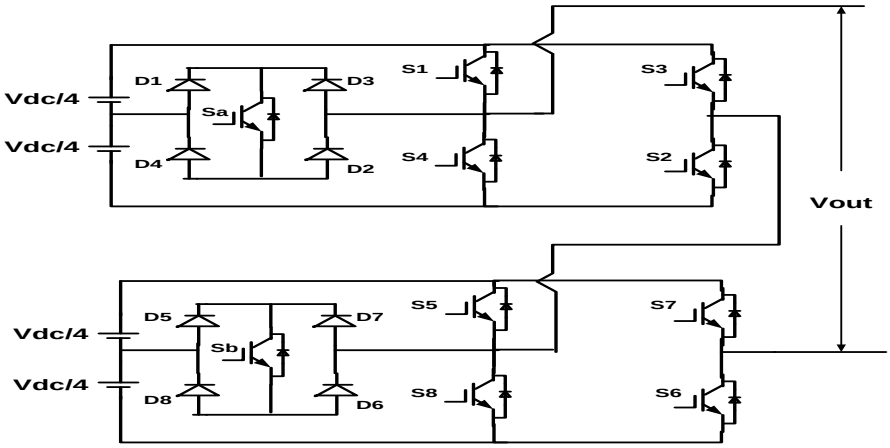

Figure 5. Cascaded Hybrid H-Bridges

The proposed CHHB uses less number of switches to produce more voltage levels. This will reduce Gate Drivers and protection circuit requirement thus it reduce cost and complexity of the circuit. For example for 9 level output the proposed converter uses 10 switches but cascaded H- Bridge converter uses 12 switches. This difference increases as the number of output voltage levels increases

Table 4 Switching table for Cascaded Hybrid H-Bridge

Switches Turn On	Voltage Level
Sa,S2,S8,D6	Vdc/4
S1.S2,S8,D6	2Vdc/4
S1,S2,Sb,S6	3Vdc/4
S1,S2,S5,S6	Vdc
S4,D2,S8,D6	0
Sa,S3,S8,D6	-Vdc/4
S3,S4,S8,D6	-2Vdc/4
S3,S4,Sb,S7	-3Vdc/4
S3,S4,S7,S8	-Vdc

III. DESIGN OF PROPOSED NOVEL HYBRID H-BRIDGE INVERTER

A. Device Current

The IGBT and DIODE currents can be obtained from the load current by multiplying with the corresponding duty cycles. Duty cycle, $d = ½(1+K m \sin\omega t)$

Where, m = modulation index K = +1 for IGBT, -1 for Diode.

$$i_{ph} = \sqrt{2}\, I\, \sin(\omega t - ø)$$

Where i = RMS value of the load (output) current,

Ø = Phase angle between load voltage and current.

Then the device current can be written as follows.

$$\therefore\ i_{device} = \frac{\sqrt{2}}{2} I \sin(\omega t - ø) * (1 + km\ \sin \omega t)$$

The average value of the device current over a cycle is calculated as

$$i_{avg} = \frac{1}{2\pi}\int_{ø}^{\pi+ø} \frac{\sqrt{2}}{2} I \sin(\omega t - ø) * (1 + k\, m sin\omega t) d\omega t$$

$$= \sqrt{2}\, I \left[\frac{1}{2\pi} + \frac{K\, m}{8} \cos ø\right]$$

The device RMS current can be written as

$$i_{rms} = \sqrt{\int_{ø}^{\pi+ø} \frac{1}{2\pi} \left(\sqrt{2}\, I \sin(\omega t - ø)\right)^2 * \frac{1}{2} * \left((1 + k\, m sin\omega t) d\omega t\right)} = \sqrt{2}\, I \sqrt{\left[\frac{1}{8} + \frac{K\, m}{3\pi} \cos ø\right]}$$

B. IGBT Loss Calculation

IGBT loss can be calculated by the sum of switching loss and conduction loss. Where conduction loss can be calculated by,

$$P_{on\,(IGBT)} = V_{ceo} * I_{avg\,(igbt)} + I^2_{rms\,(igbt)} * r_{ceo}$$

$$I_{avg\,(igbt)} = \sqrt{2}\, I \left[\frac{1}{2\pi} + \frac{m}{8} \cos ø\right]$$

$$I_{rms\,(igbt)} = \sqrt{2}\, I \sqrt{\left[\frac{1}{8} + \frac{m}{3\pi} \cos ø\right]}$$

Values of V_{ceo} and r_{ceo} at any junction temperature can be obtained from the output characteristics (Ic vs. Vce) of the IGBT as shown in Fig .6.

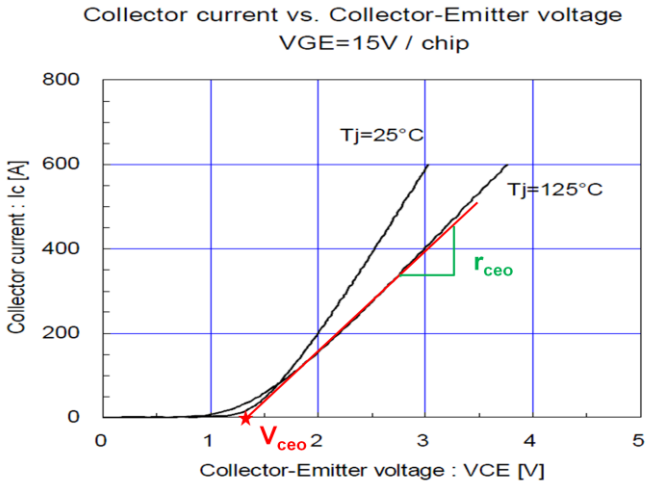

Figure 6 IGBT output characteristics

The switching losses are the sum of all turn-on and turn-off energies at the switching events

$$E_{sw} = E_{on} + E_{off} = a + b\, I + c\, I^2$$

Assuming the linear dependence, switching energy $E_{sw} = (a + b\, I + c\, I^2) * \frac{V_{DC}}{V_{nom}}$

Here V_{DC} is the actual DC-Link voltage and V_{nom} is the DC-Link Voltage at which E_{sw} is given. Switching losses are calculated by summing up the switching energies.

$$P_{sw} = \frac{1}{T_o} \sum_n E_{sw}\,(i)$$

Here 'n' depends on the switching frequency.

$$P_{sw} = \frac{1}{T_o} \sum_n (a + b\, I + c\, I^2)$$

$$= \frac{1}{T_o} \left[\frac{a}{2} + \frac{b\, I}{\pi} + \frac{c\, I^2}{4}\right]$$

After considering the DC-Link voltage variations switching losses of the IGBT can be written as follows.

$$P_{sw\,(IGBT)} = f_{sw} \left[\frac{a}{2} + \frac{b\, I}{\pi} + \frac{c\, I^2}{4}\right] * \frac{V_{DC}}{V_{nom}}$$

So, the sum of conduction and switching losses gives the total losses.

$$P_{T\,(IGBT)} = P_{on\,(IGBT)} + P_{sw\,(IGBT)}$$

C. Diode Loss Calculation

The DIODE switching losses consists of its reverse recovery losses and the turn-on losses are negligible.

$$E_{rec} = a + b\,I + c\,I^2$$

$$P_{sw\,(DIODE)} = f_{sw}\left[\frac{a}{2} + \frac{b\,I}{\pi} + \frac{c\,I^2}{4}\right] * \frac{V_{DC}}{V_{nom}}$$

So, the sum of conduction and switching losses gives the total DIODE looses.

$$P_{T\,(DIODE)} = P_{on\,(DIODE)} + P_{sw\,(DIODE)}$$

The total loss per one switch (IGBT+DIODE) is the sum of one IGBT and DIODE loss.

$$P_T = P_{T\,(IGBT)} + P_{T\,(DIODE)}$$

D. Thermal Calculations

The junction temperatures of the IGBT and DIODE are calculated based on the device power losses and thermal resistances. The thermal resistance equivalent circuit for a module is shown in Fig 7. In this design the thermal calculations are started with heat sink temperature as the reference temperature. So, the case temperature from the model can be written as follows.

$$T_c = P_T\,R_{th(c-h)} + T_h$$

Here $R_{th(c-h)}$ = Thermal resistance between case and heat sink

P_T = Total Power Loss (IGBT+DIODE)

IGBT junction temperature is the sum of the case temperature and temperature raise due to the power losses in the IGBT.

$$T_{j\,(IGBT)} = P_{T(IGBT)}\,R_{th(j-c)IGBT} + T_c$$

DIODE junction temperature is the sum of the case temperature and temperature raise due to the power losses in the DIODE.

junction temperatures. In order to make the calculated values close to the actual values,

$$T_{j\,(DIODE)} = P_{T(DIODE)}\,R_{th(j-c)DIODE} + T_c$$

The above calculations are done based on the average power losses computed over a cycle. So, the corresponding thermal calculation gives the average junction temperatures. In order to make the calculated values close to the actual values,

transient temperature values are to be added to the average junction temperatures.

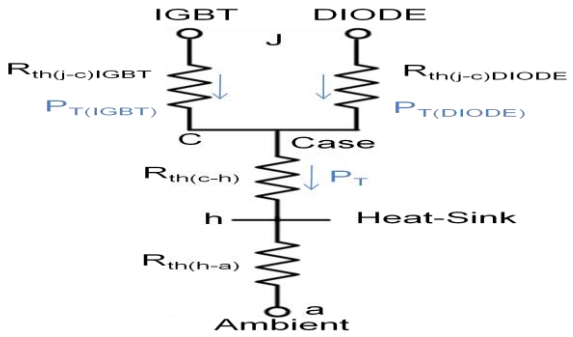

Figure. 7 Thermal resistance equivalent circuit

E. DC-Capacitor Selection

The required capacitance for each cell depends on the allowable ripple voltage and the load current. The rms ripple current flowing into the capacitor can be written as follows and the ripple current frequency is double the load current frequency (Hybrid H-Bridge).

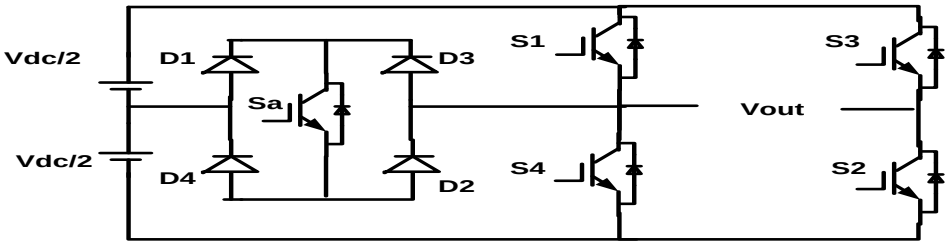

Figure. 8 Hybrid H- Bridge converter

$$I_c = -\frac{I}{V_{dc}}\frac{1}{2}\left(|U_{ac}| * K + I\omega L\right)\sin(2\omega t)$$

Since the value of 'L' is very small, the above equation can be written as below.

$$I_c = -\frac{I}{V_{dc}}\frac{1}{2}\left(|U_{ac}| * K\right)\sin(2\omega t)$$

$$I_C = -K\frac{1}{2}\frac{|U_{ac}|}{V_{dc}} * \sin(2\omega t) = -K\frac{m}{2}\sin(2\omega t)$$

Here 'm' is the modulation index.

$$\text{Here } I_{cp} = C\frac{du_{pp}}{dt}$$

$$\frac{m}{2} I\sqrt{2} = \mathrm{C}\, 2\omega * \Delta V\ V_{dc}$$

$$\mathrm{C} = \frac{m}{4\omega}\frac{1}{\Delta V\, V_{dc}}\sqrt{2}\, I$$

IV. PROPOSED PV SYSTEM

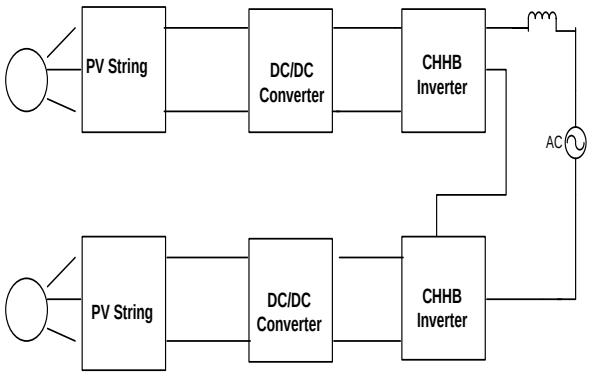

Figure. 9. Grid Connected PV System

The general block diagram of PV system is shown here. The PV string converters solar radiation into DC.Here we are using DC/DC Boost converter to increase the output voltage. The output inverter converts DC into AC and feeding into the grid. The proposed system uses small PV array cascading to produce higher voltage output. This system reduces overall cost and complexity. The Fig.8 shows the proposed PV configuration.

V. SIMULINK MODELING AND SIMULATION RESULTS

Fig. 10 Shows the Matlab/Simulink model of complete PV system. It consists of PV array block, DC/DC converter Block, Hybrid H-Bridge Block.

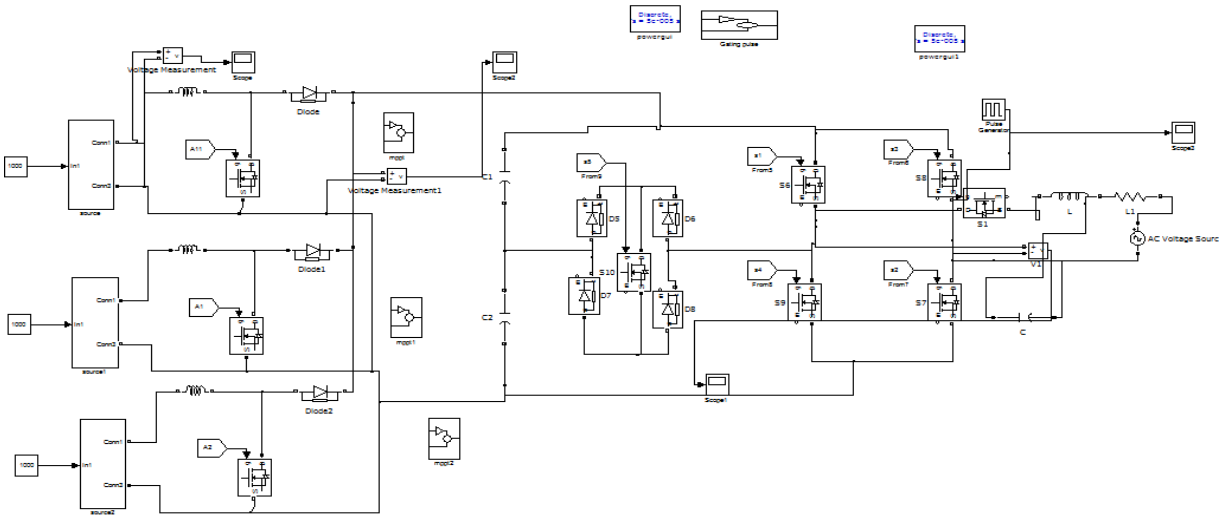

Figure. 10 Matlab/Simulink model of Hybrid H-bridge

Fig. 11 shows the inverter input DC voltage and Multilevel AC output voltage. Fig. 12 Shows the five level output of the Hybrid H-Bridge. Fig.13 shows the grid voltage and current wave forms.

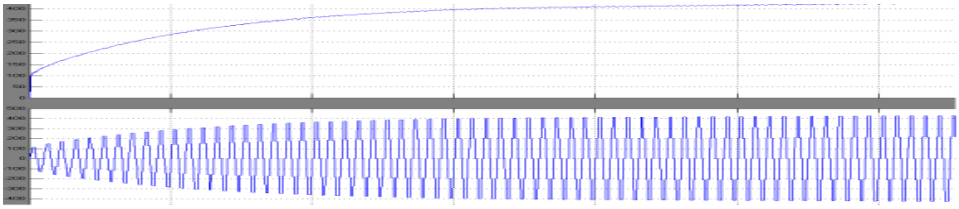

Figure.11 Inverter Input and Output

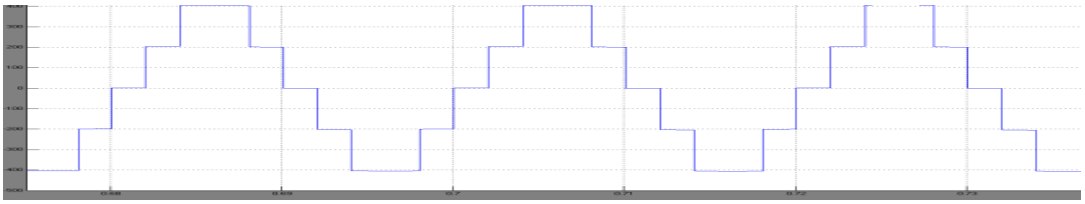

Figure12. Five level output of Hybrid H-bridge

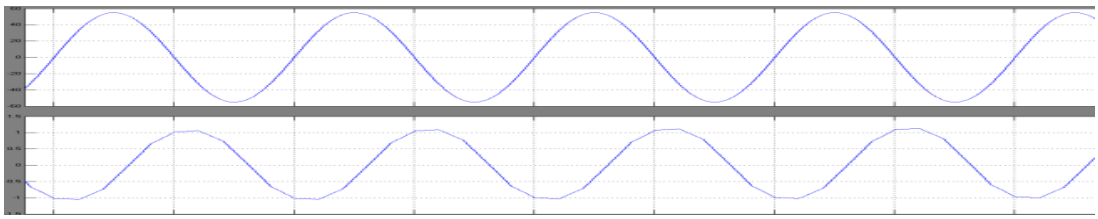

Figure13 Gr**id voltage and Grid current**

VI. CONCLUSION

This paper presents a single-phase multistring Multi-level photovoltaic (PV) inverter topology for grid-connected PV systems with a novel hybrid H- bridge inverter. The proposed novel cascaded Hybrid H-bridge produces higher voltage levels with less number of devices. This will reduce the number of gate drivers and protection circuits requirement, this inurn reduces the cost increase the reliability. Design Procedure for various components of single Hybrid H- bridge cell is given. A cascaded Grid connected PV topology is proposed. Finally a Matlab/Simulink based model is developed and simulation results are presented.

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