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Design and Simulation of Low Power 6TSRAM and Control its Leakage Current Using Sleepy Keeper Approach in different Topology

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Abstract : *Today, low power memory is given most priority in VLSI design. The power is most important aspect for today's technology. So the power reduction for one cell is the vital role in memory design techniques. As the technology growing portable device (e.g. Cell phone, PDA) increases, the Static Power Consumption (Leakage Power) became a significant issue. Leakage current in standby mode is the major part of power loss. We concentrate on the technique that to reduce the leakage current in standby mode. The one CMOS transistor leakage current due to various parameters is the essentiel role of power consumption. The CMOS leakage current to the process level can be decreased by using sleepy keeper technique. The advantages in this technique are ultra-low leakage with dual Vth, state-saving, less area penalty and faster than other techniques like sleepy stack approach, sleep, Zig Zag.*

This project's focus is to reduce leakage power consumption of an 6TSRAM by employing Sleepy Keeper technique in different topology.

Keywords: *CMOS, Leakage current, sleep, Sleepy Stack, Sleepy Keeper, SRAM, Threshold Voltage*

I. INTRODUCTION

Semiconductor memory technology is an essential element of today's electronics. Normally based around semiconductor technology, memory is used in any equipment that uses a processor of one form or another. Indeed as processors have become more popular and the number of microprocessor controlled items has increased so has the requirement for semiconductor memory. An additional driver has been the fact that the software associated with the processors and computers has become more sophisticated and much larger, and this too has greatly increased the requirement for semiconductor memory. In view of the pressure on memory, new and improved semiconductor memory technologies are being researched and development can be very rapid. Nevertheless, the more mature semiconductor memory technologies are still in widespread use and will remain so for many years to come. In addition to these new applications such as digital cameras, PDAs and many more applications have given rise to the need to memories. Accordingly it is not uncommon to see semiconductor memories of 8 Gigabyte and much more required for various applications. With the rapid growth in the requirement for semiconductor memories there have been a number of technologies and types of memory that have emerged. Names such as ROM, RAM, EPROM, EEPROM, Flash memory, DRAM, SRAM, SDRAM, and the very new MRAM can now be seen in the electronics literature. Each one has its own advantages and area in which it may be used.[1][2]

Previously many works had been done in the field of Leakage Current reduction using different techniques like Sleep, Sleep, Zigzag, Stack, Sleepy-Stack, Leakage feedback in different circuits.

Here we present a new VLSI technique to reduce leakage power, the Sleepy Keeper Technique provides an efficient way to reduce leakage power, but disadvantage of this technique increase the delay as the transistor are increased. In this paper 6TSRAM cell was designed with Sleepy Keeper technique and analyze the Leakage, Dynamic power consumption and Static power consumption in different topology.

II. LEAKAGE CURRENT

With the rapid progress in semiconductor technology, chip density and operation frequency have increased, making the power consumption in battery-operated portable devices a major concern. High power consumption reduces the battery service life. IC power dissipation consists of different components depending on the circuit operating mode. First, the switching or dynamic power component dominates during the active mode of operation. Second, there are two primary leakage sources, the *active* component and the *standby* leakage component. The standby leakage may be made significantly smaller than the active leakage by changing the body bias conditions or by power-gating.

There are four main sources of leakage current in a CMOS transistor (Fig 1): Reverse-biased junction leakage current (IREV), Gate induced drain leakage (IGIDL), Gate direct-tunneling leakage (IG), Sub threshold (weak inversion) leakage (ISUB). [3]

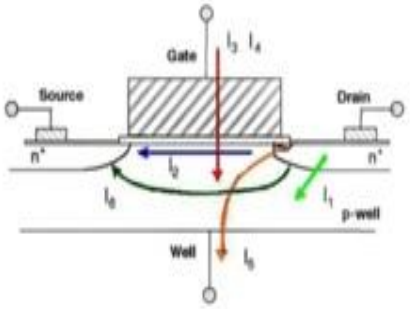

Fig.1Source of Leakage Current in CMOS Transistor

III. Method of Controlling Leakage Power

Dynamic power has been a predominant source of power dissipation recently. However, static power dissipation is becoming a significant fraction of the total power. Leakage power has become a top concern to the field of VLSI. The leakage problem is worse than generally thought because the simple, traditional leakage power estimation of multiplying the average transistor leakage. Leakage power has become a top concern for IC designers in deep submicron process technology nodes 65nm and below. Leakage power is primarily the result of unwanted sub threshold current through the transistor channel when the transistor is turned off. Here some methods that are already used to control the leakage power are Sleep, Zigzag, Stack, Sleepy-Stack, Leakage feedback.

The most well-known traditional approach is the sleep approach [2][3]. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. Fig 3 shows its structure. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively.

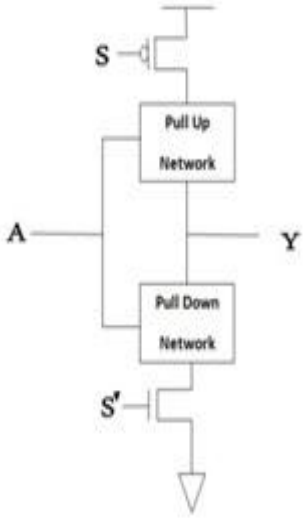

Fig. 2 Sleepy Approach

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [5]. Fig 4 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub-threshold leakage current reduction.

The sleepy stack approach combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach [6][7]. Then sleep transistors are added in parallel to one of the divided transistors. Fig 3 shows its structure. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode.

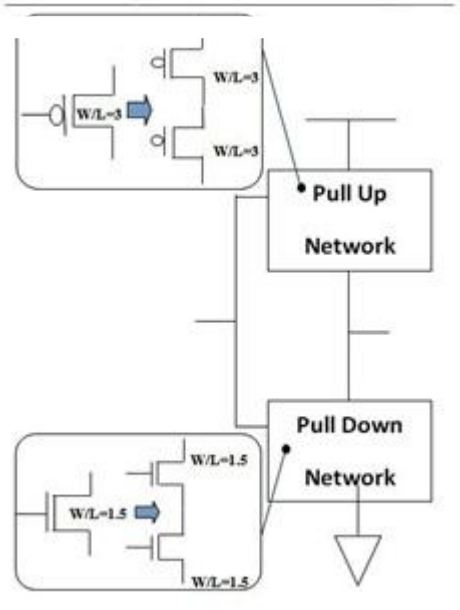

Fig.3 Stack Approach

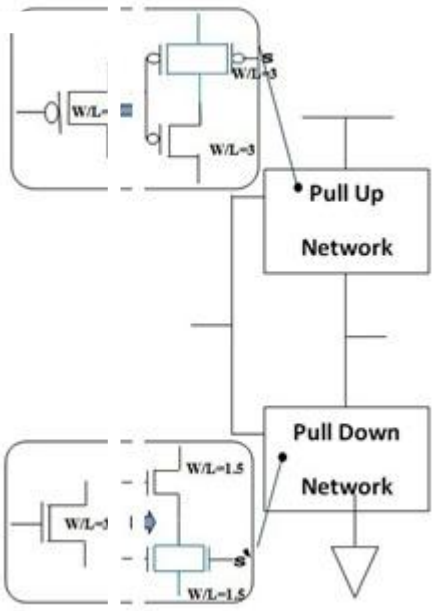

Fig.. Sleepy Stack Approach

The leakage feedback approach is based on the sleep approach. However, the leakage feedback approach uses two additional transistors to maintain logic state during sleep mode, and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback [7]. As shown in Fig.6, a PMOS transistor is placed in parallel to the sleep transistor (S) and a NMOS transistor is placed in parallel to the sleep transistor (S'). The two transistors are driven by the output of the inverter which is driven by the output of the circuit. During sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail.[4][5][6][7]

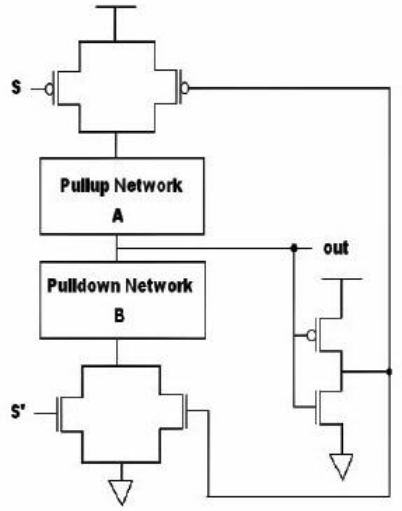

Fig. 5 Leakage Feedback Approach

IV. PROPOSED APPROACH: SLEEPY KEEPER

In this section, we describe our new leakage reduction technique, which we call the "sleepy keeper" approach. This section explains the structure of the sleepy keeper approach as well as how it operates. The basic problem with traditional CMOS is that the transistor are used only in their most efficient, and naturally inverting way namely, PMOS transistor connected to V_{dd} and NMOS transistors connected to is GND. It is well known that pMOS transistors are not efficient at passing GND; similarly it is well known that NMOS transistors are not efficient at passing V_{dd}. However to maintain '1' in sleep mode, given that the value '1' valued has already been calculated, the sleepy keeper approaches uses this output value '1' and an NMOS transistor connected to V_{dd} to maintain output value equal to '1' when in sleep mode. For example, when the output is '1' for an inverter design utilizing the sleepy keeper approach, the current path is shown in the figure, similarly to maintain a value of '0' in sleep mode, given that the '0' value has already be calculated, the sleepy keeper uses this output value of '0' and the p MOS transistor connected to ground to maintain output value equal to '0' when in sleep mode. For example when the output is '0' for an inverter implemented using the sleepy keeper approach, the current path is shown in Fig.6 [7][8][9].

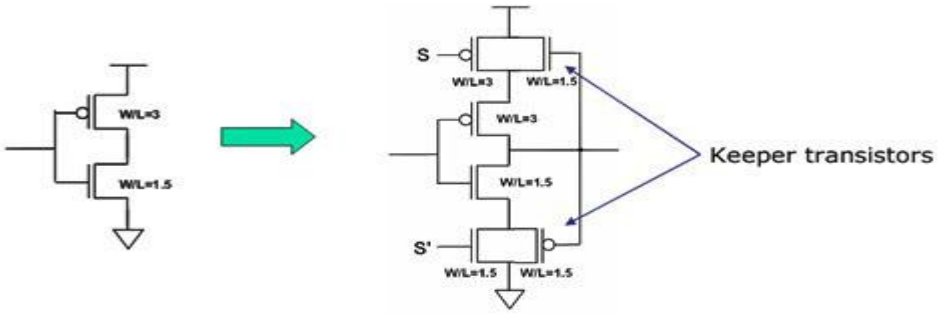

Fig.6 CMOS Inverter to Sleepy Keeper Inverter

V. SRAM

SRAM or Static random Access memory is a form of semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, and does not need to be dynamically updated. While the data in the SRAM memory does not need to be refreshed dynamically. Static random access memory (SRAM) is a type of volatile semiconductor memory to store binary logic '1' and '0' bits. SRAM uses bi stable latching circuitry made of Transistors MOSFETS to store each bit. When the cell is chosen, the value to be written is stored in the cross-coupled flip-flops. A basic SRAM cell consists of two cross coupled inverters forming a simple latch as storage elements and two switches connecting these two inverters to complementary bit lines to communicate with the outside of the cell.

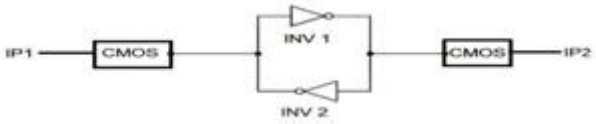

Fig.7 Cross Coupled inverter SRAM cell

VI. 6TSRAM

The schematic of SRAM cell is shown in the Fig.8. It has 2 pull up PMOS and 2 NMOS pull down transistors as two cross coupled inverters and two 2 NMOS access transistors to access the SRAM cell during Read and Write operations. Both the bit lines (BL and BLB) are used to transfer the data during the read and write operations in a differential manner. Bit 0 or 1 in a SRAM cell is stored using two cross coupled inverters. This storage cell has two stable states **0** and **1** which is reinforced because of cross coupling. Two additional *access* transistors serve to control the access to the storage cell during read and write operations. So a typical SRAM cell is a six transistor structure. A 6T SRAM cell requires a careful device sizing to ensure read stability, write margin and data retention in standby modes. Access to the cell is enabled by the word line which controls the two access transistors M5 and M6. They in turn control whether the cell should be connected to the bit lines. Bit lines are used for both read and write operations. Two bit lines are not necessary but they are provided to improve noise margins. In read stability, M1 transistor is required to be much larger than M5 transistor to make sure that the node between M1 and M5 does not flip. In write mode, bit lines overpower cell with a new value. High bit lines must not overpower inverters during read operation.

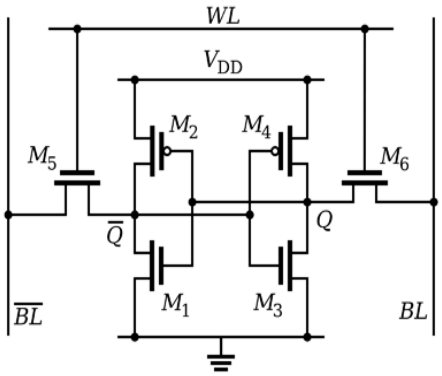

Fig.8 6T SRAM

Read Operation:

The read cycle starts by pre-charging both the bit lines to a logical 1 and then asserting the word line, enabling both the access transistors. If a 1 is stored in the cell, this value is transferred to the bit lines by leaving BL (bit line) at its pre-charged value and discharging BLB to a logical 0 through M1 and M5. The transistors M4 and M6 pull the bit line to a logical 1. If the content of the memory is a 0, then BL is pulled to a logical 0 and BLB to a logical 1.

Write Operation:

If a 0 is to be written, BL and BLB are set to 0 and 1 respectively. A 1 is written by inverting the values of the bit lines. WL (word line) is then asserted and the value that is to be stored is latched in.

VII. DESIGN AND SIMULATION

We have design simple 6TSRAM and 6TSRAM with Sleepy Keeper approach in different technology, the schematic and layouts are designed using Microwind.

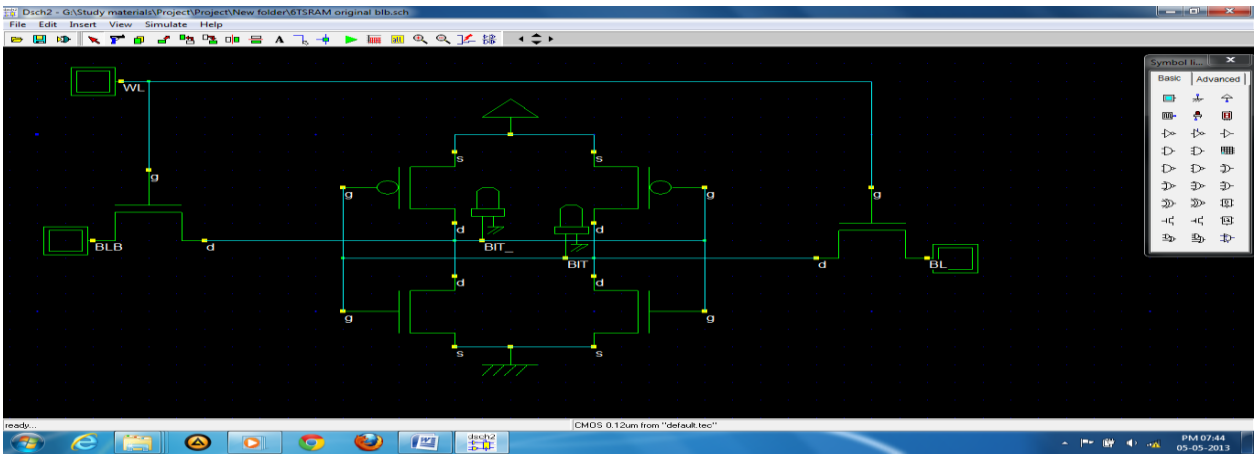

Fig.9 Basic 6TSRAM Cell

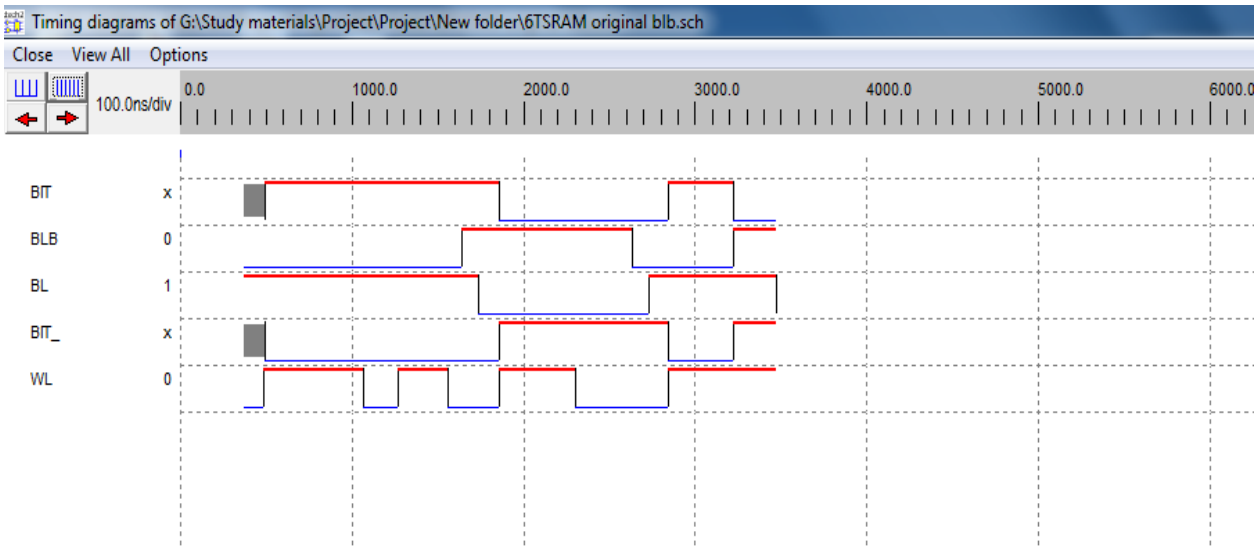

Fig.10 Simulation Result of Basic 6T SRAM cell

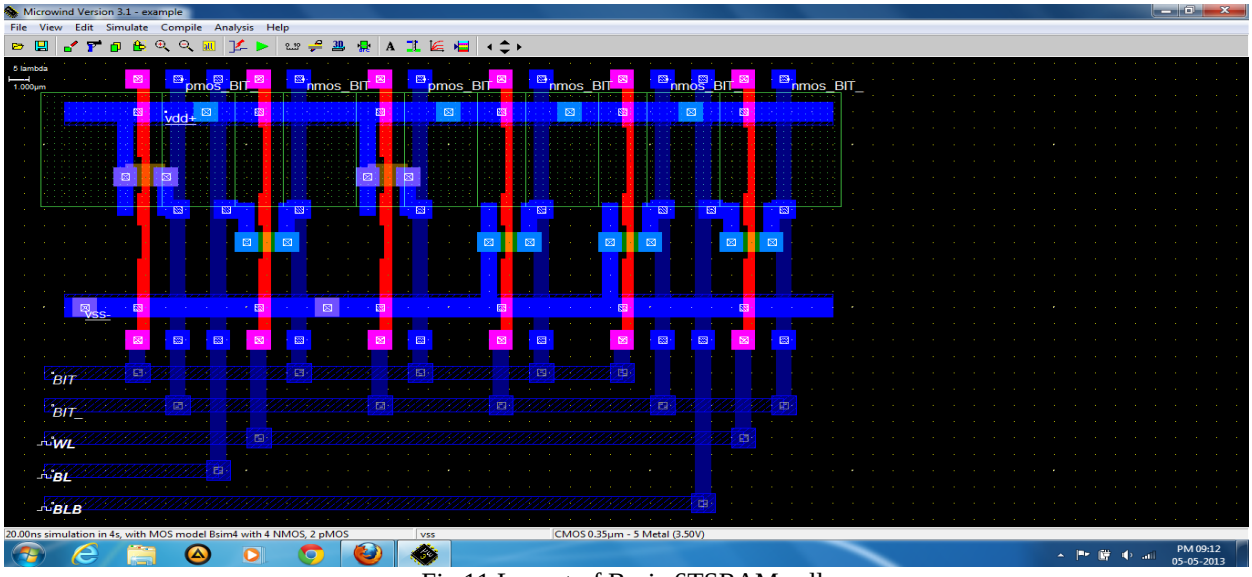

Fig.11 Layout of Basic 6TSRAM cell

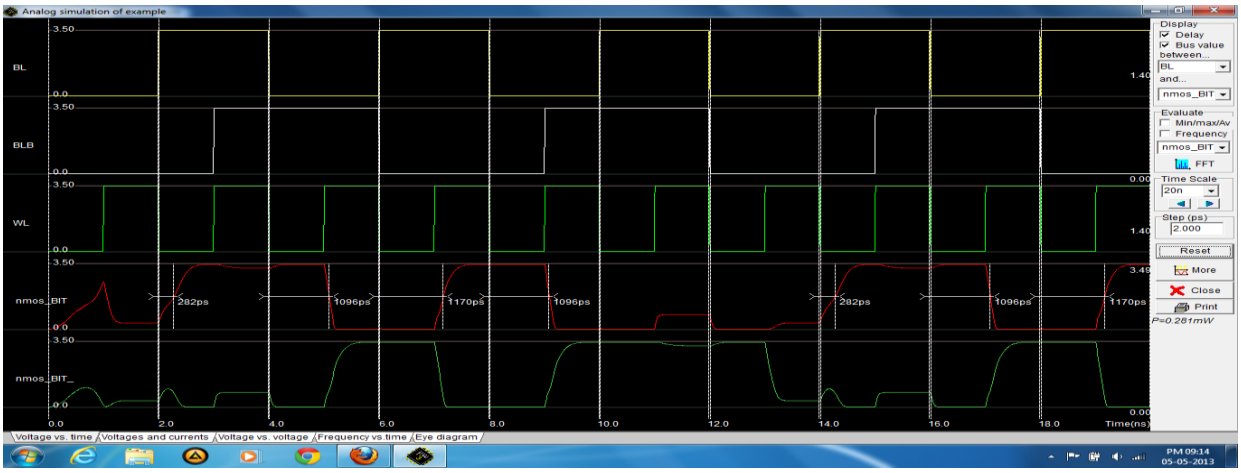

Fig.12 Output of basic 6TSRAM

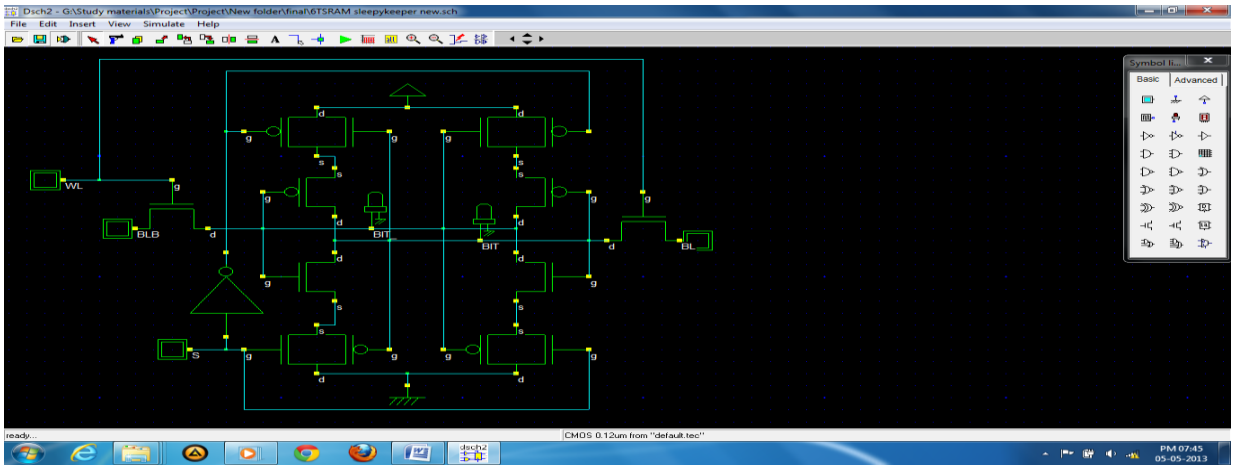

Fig.13 6TSRAm cell using Sleepy Keeper Approach

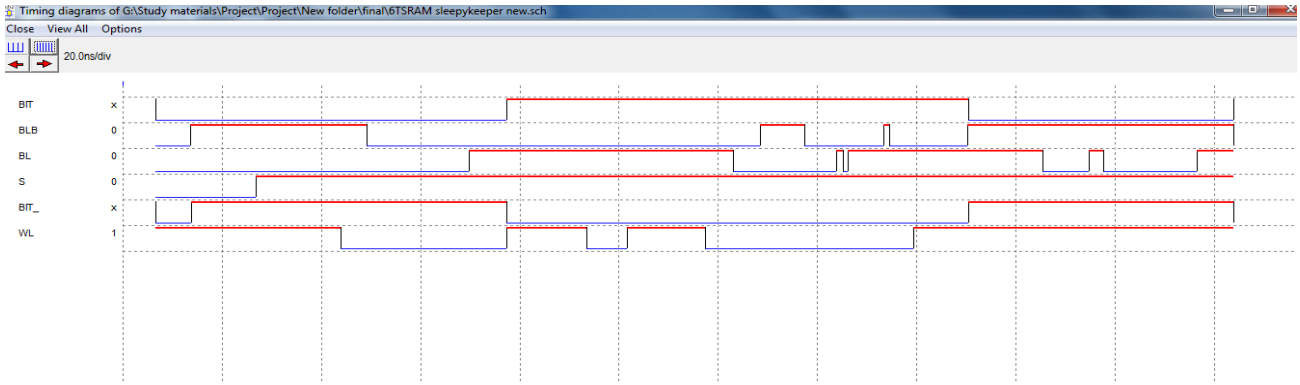

Fig.14 Simulation result of 6TSRAM with Sleepy Keeper Approach

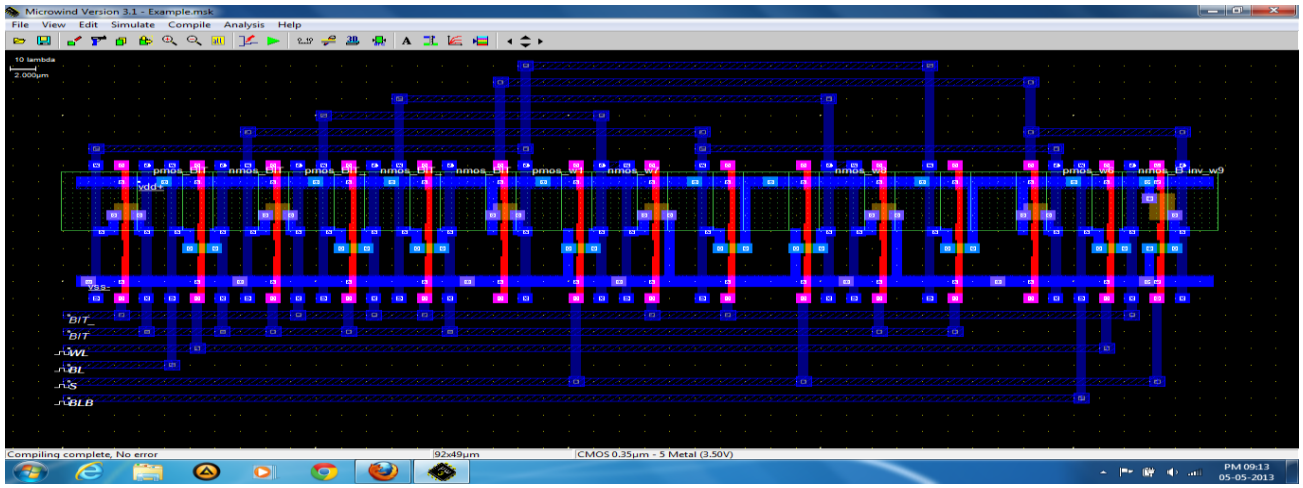

Fig.14 Layout of 6TSRAM using Sleepy Keeper Approach

Comparison between Basic 6TSRAM and 6TSRAM using sleepy Keeper Approach

Topology	Basic SRAM (W)	SRAM using Sleepy Keeper approach (W)
350 nm	270 E-06	90 E-06
250 nm	178 E-06	62 E-06
180 nm	108 E-06	43 E-06
120 nm	96 E-06	37 E-06
65 nm	36 E-06	13 E-06

Table 1. Power consumption of basic 6TSRAM and SRAM using Sleepy Keeper Technique

VIII. CONCLUSION

In this paper we design 6TSRAM by using the "Sleepy Keeper" leakage current reduction technique. The proposed circuits were designed in 65, 120, 180, 250, 350 nanometer CMOS/VLSI technology. In this paper we observed that the proposed technique "Sleepy Keeper" have low power consumption when compared to the other low power techniques and

having delay and area overhead. Based on simulations result with a SRAM Architecture circuit, we find that "Sleepy Keeper approach" achieves up to 65 % less power consumption. Hence it is concluded that the proposed 6TSRAM is used for low power designs and these designed techniques are used for high performance and low power applications.

IX. ACKNOWLEDGEMENTS

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