International Journal of Modern Engineering Research (IJMER)
www.ijmer.com Vol. 3, Issue. 6, Nov - Dec. 2013 pp-3646-3648 ISSN: 2249-6645

Application of CNTFET as Logic Gates and its implementation using HSPICE

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Abstract: *The steady reduction in the dimension of transistors, according to Moore's law has been the main force behind the regular leaps in the level of performance of the silicon ICs. Due to the effects like the short channel effects, tunnelling effect, additional heat dissipation, interconnect problems etc problems arise. So it is not possible to reduce the size further. Hence now it is necessary to adopt new material or technology. Carbon Nano Tube Field Effect Transistors (CNTFETs) are being widely studied as possible successors to silicon MOSFETs. This paper focuses on simulation of CNTFET based digital circuits using HSPICE and parameters like delay, power and PDP are calculated.*

Keywords: *Avanwaes, Carbon Nanotube, Carbon Nanotube Field Effect Transistor, Logic gates, Top gated transistor.*

I. Introduction

For many years MOSFET has been used as a basic element of circuit designing [1]. As the miniaturization of silicon based circuits reaches its physical limitations scientists are trying to adopt new material or technology which preserve a lot of what's good about existing silicon technology and also cope up with the problem associated with physical limits. CNTFET is a novel device that is projected to outperform scaled CMOS technologies. CNTFET-based devices offer high mobility for near-ballistic transport, high carrier velocity for fast switching. HSPICE compatible CNT model is used to design digital circuits and simulation is done on Avanwaves. In this paper, section II Introduces the Carbon nanotubes, section III delves into the CNTFET and model which is used. Simulation results and parameter calculation of digital circuits are in section IV. Finally, Sections V discuss the conclusion and future scope.

II. Carbon Nanotube (CNT)

The first person to see carbon nanotubes was Sumio Iijima of NEC Crop in Tokyo, who discovered them in 1991 while studying electron microscope images of the soot produced by electrical discharges between carbon electrodes. Carbon nanotubes are basically hollow cylinders with diameters ranging from 1 nm to 50 nm and length, over 10µm [2]**.** The carbon atoms are arranged into hexagons that form a honeycomb pattern. A nanotube can be viewed as a single layer or multilayer of graphite rolled into a seamless cylinder, as shown in Fig. 1. There are two types of nanotubes; one is a single-wall nanotube (SWCNT) that is made up of a single layer of graphite ("graphene" sheet), and the other is a multiwall nanotube (MWCNT) that consists of multiple shells [3].

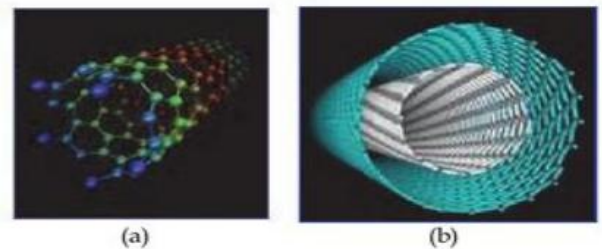

Figure 1: Structure models of nanotubes (a) SWCNT (b) MWCNT

The way that graphene is rolled is described by a pair of indices (n, m), which are called "chiral vector". According to the chiral vector of a CNT, it can be determined whether it's a metallic or semiconducting CNT.

III. Carbon Nanotube Field Effect Transistor (CNTFET)

A single carbon nanotube is positioned as a bridge between two electrodes. The electrodes became the source and drain of the transistor, and the nanotube played the role of the channel, as shown in the schematic Fig. 2.

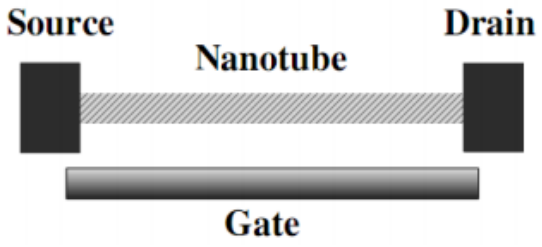

Figure 2: Schematic of CNTFET

Applying the appropriate voltage to gate the nanotube is on or off. The first carbon nanotube field-effect transistors (CNTFETs) were reported in 1998. In the nanotube device, the transistor action occurs at the contact points between the metal electrodes and the carbon nanotube. Semiconducting CNTs have been used to fabricate CNTFETs, which show promise due to their superior electrical characteristics over silicon based MOSFETs [4]. In terms of the device operation mechanism, CNFET can be categorized as either Schottky Barrier (SB) controlled FET or MOSFET-like FET. The ambipolar behaviour of SB-controlled CNFET makes it undesirable for complementary logic design. Considering both the fabrication feasibility and superior device performance of the MOSFET-like CNFET as compared to the SB-controlled FET, **we choose to focus on MOSFET-like CNFETs in this work.** The complete CNFET device model [5, 6] which is used is implemented hierarchically in three levels. Device nonidealities are included hierarchically at each level. The summary of model which is used is given in the table below.

Device Types	n-type/p-type CNFET
Device Dimensions:	
Channel Length (Minimum)	~10nm
Channel Length (Maximum)	Unlimited
Channel Width (Minimum)	4nm
Channel Width (Maximum)	Unlimited
Number of CNTs / device (Minimum)	1
Number of CNTs / device (Maximum)	Unlimited

Table 1: Summary of the CNFET Model

32nm technology with (19, 0) semiconducting with 1.5nm diameter CNT is used. The supply given is 0.9V and gate and drain voltage can be varied upto supply voltage i.e. 0.9V.

IV. SIMULATION RESULT

The logic gates like AND gate, OR gate, EXOR gates are simulated. Their output characteristics are plotted. All the following circuits are simulated at room temperature and the supply voltage is 0.9V. For all circuits a 10 femto Farad load capacitor has been used. Delay, Power and PDP calculations are also done for these logic gates.

The AND gate performs logical multiplication, the AND gate shown in Fig. 3 If A and B are two inputs, then output Y can be represented mathematically as F = A.B, here dot (.) denotes the AND operation. Fig. 4 shows the behaviour of output of AND gate is HIGH only when all its inputs are AND gate. Table 2 shows variations in delay and average power for AND gate on varying the supply voltages.

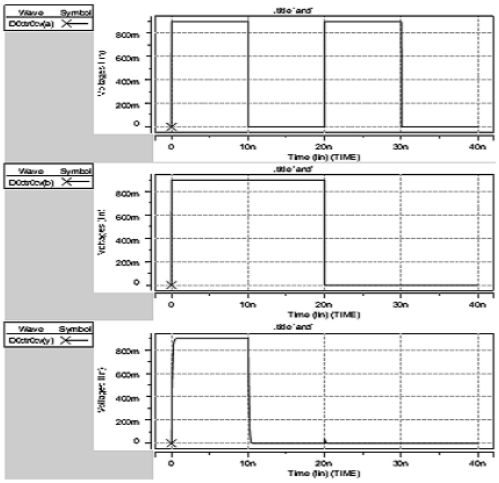

Figure 4: characteristics of CNTFET-AND gate

Figure 3: symbol of AND gate

SUPPLY (V)	AND GATE		
	DELAY (sec)	POWER (W)	PDP (J)
0.9	8.639e-11	1.840e-06	1.589e-16
0.8	7.711e-11	1.500e-06	1.156e-16
0.65	6.319e-11	1.065e-06	6.729e-17

Table 2: AND gate simulation results

The OR gate performs logical addition, the OR gate shown in Fig. 5.The output of OR gate is HIGH only when any one of its inputs are high. If A and B are two inputs, then output Y can be represented mathematically as Y = A+B. Fig. 6 shows the behaviour of output of OR gate is HIGH when any or both of its inputs are high. Table 3 shows variations in delay and average power for OR gate on varying the supply voltages.

Figure 5: symbol of OR gate

SUPPLY (V)	OR GATE		
	DELAY (sec)	POWER (W)	PDP (J)
0.9	8.451e-11	1.830e-06	1.546e-16
0.8	7.349e-11	1.490e-06	1.095e-16
0.65	6.022e-11	1.055e-06	6.353e-17

Table 3: OR gate simulation results

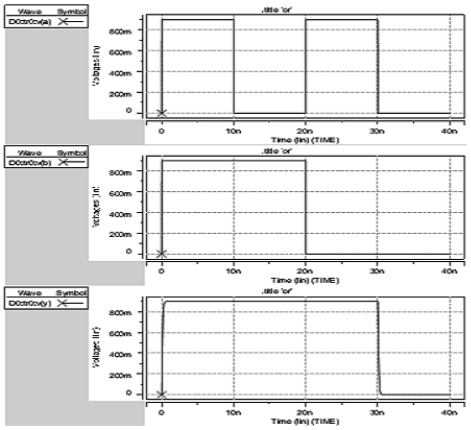

Figure 6: characteristics of CNTFET-OR gate

An Exclusive-OR (XOR) gate is gate shown in Fig. 7 with two inputs and one output. The output of a two-input XOR gate assumes a HIGH state if one and only one input assumes a HIGH state. If A and B are two inputs, then output Y can be represented mathematically as Y = A'B+AB'. Fig. 8 shows the behaviour of output of XOR gate is HIGH when only one of its inputs is high. Table 4 shows variations in delay and average power for EXOR gate on varying the supply voltages.

Figure 7: symbol of EXOR gate

SUPPLY (V)	EXOR GATE		
	DELAY (sec)	POWER (W)	PDP (J)
0.9	1.019e-08	1.839e-06	1.873e-14
0.8	1.017e-08	1.499e-06	1.524e-14
0.65	1.014e-08	1.064e-06	1.078e-14

Table 4: EXOR gate simulation results

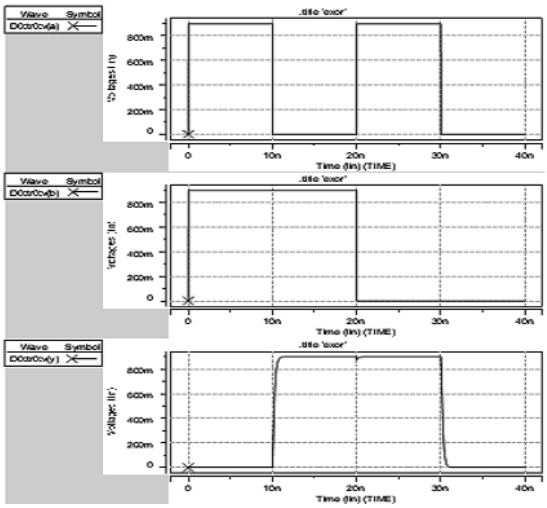

Figure 8: characteristics of EXOR gate

V. Conclusion And Future Scope

Unipolar, MOSFET like CNTFET model is used to implement various digital circuits like AND,OR, EXOR gates. This model is used for designing digital circuits whose coding has been done in HSPICE, the output waveform is displayed on AvanWaves and delay, average power calculations have been done for these digital circuits for various value of supply i.e. 0.9, 0.8, 0.65 V.

Complex digital circuits based on CNTFET technology can be designed using these basic gates and a comparative study can be done with that of Silicon technology.

REFERENCE

[1] P. Avouris, "Super tubes." IEEE Spectrum, pp. 41-45, Aug 2004.
[2] Y.M. Lin et al., "High-Performance Carbon Nanotube Field-Effect Transistor With Tunable Polarities", IEEE Trans. on Nanotech, Vol. 4, No. 5, pp. 481-489, 2005.
[3] Y. Saito, "Preparation and Properties of CNT," International Symposium on micromechatronics and human science, pp.43-49,1999.
[4] Ali Keshavarzi, Arijit Raychowdhury, Juanita Kurtin, Kaushik Roy, and Vivek De, "Carbon Nanotube Field-Effect Transistors for HighPerformance Digital Circuits—Transient Analysis, Parasitic, and Scalability", IEEE Transactions On Electron Devices, Vol. 53, NO. 11, Nov-2006.
[5] C. Dwyer, M. Cheung and D. J. Sorin, "Semi empirical SPICE models for carbon nanotube FET logic," in Proc. Conf. Nanotechnology, Aug. 2004, pp. 386–388.
[6] Fabien Pregaldiny et.al.,―Compact Modelling and Applications of CNTFETs for Analog and Digital Circuit Design, IEEE Trans. Elec.dev., pp. 1030–1033, 2006.