OPEN ACCESS

International
Journal
Of Modern Engineering Research (IJMER)

Optimized FIR filter design using Truncated Multiplier Technique

V. Bindhya[1], R. Guru Deepthi[2], S. Tamilselvi[3], Dr. C. N. Marimuthu[4]

[1] *M.E Applied Electronics, Department of ECE, Nandha Engineering College, Erode.*
[2]*M.E Vlsi design, Department of ECE, Nandha Engineering College, Erode.*
[3]*M.E Vlsi design, Department of ECE, Nandha Engineering College, Erode.*
[4]*DEAN, Department of ECE, Nandha Engineering College, Erode*

ABSTRACT: *In this paper we have proposed an efficient way of FIR filter design using truncated multiplier technique. The Multiplication operation is performed using Multiple Constant Multiplication Accumulation Truncation (MCMAT) technique. The proposed multiplier design is based on the Wallace tree compressor (WTC). As a result it offers significant improvements in area, delay and power when compared with normal Carry Propagation Addition (CPA). Usually the product of two numbers appears as output in the form of LSB and MSB. The LSB part is truncated and compressed using MCMAT technique. The proposed design produces truncation error which is not more than 1 ulp (unit of least position). While implementing the proposed method experimentally, there is no need of any error compensation circuits and the final output is precised. Hence the area can be saved and the power is also reduced.*

Keywords: *Digital signal processing (DSP), Finite Impulse Response (FIR) filter, Multiple constant Multiplication Accumulation Truncation (MCMAT), Truncated multipliers, WTC.*

I. Introduction

Digital signal processing (DSP) is one of the core technologies in multimedia and communication systems. Most of Digital signal processing (DSP) needs faster multiplication and addition operations to be performed. Multiplication is frequently required in digital signal processing for filter realization. Many research works deals with the low power design of high speed multipliers. Since the multipliers have a significant impact on the performance of the entire system, many high-performance algorithms and architectures have been proposed to accelerate multiplication [3]. Filtering is an operation usually performed to extract the needed information from a digital signal. A signal/data stored in memory contains both wanted and unwanted information (noise). On the basis of impulse response, there are two fundamental types of digital filters: Infinite Impulse Response (IIR) filters, and Finite Impulse Response (FIR) filters. Finite Impulse Response digital filter has strictly exact linear phase, relatively easy to design, highly stable, computationally intensive, less sensitive to finite word-length effects, arbitrary, amplitude-frequency characteristic and real-time stable signal processing requirements etc.FIR filter is described by differential equation. The output signal is a convolution of an input signal and the impulse response of the filter.

$$y(n) = \sum_{k=0}^{N-1} (h(k)\ x(n-k)) \qquad (1)$$

where x(n) is the input signal.
h(n) is the impulse response of FIR filter.

Normally, multiplication involves two basic operations as partial production generation and their partial product summation. The main bottle-neck of the area is in the multiplication of two numbers as it generates a product with twice the original bit width.. The critical path for the multiplier is on the number of partial products. The partial products generated are added using Wallace Tree Compressor (WTC).The basic idea of this work is to use WTC instead of CPA to achieve lower area and power consumption. The main advantage of this WTC logic reduces the number of full adders and half adders during the tree reduction. The design achieves less area and power which leads to have truncation error of not more than 1 ulp (unit of least position). So there is no need of error compensation circuits hence the final output will be précised.

This paper is organized as follows. In Section II, discusses the MCMAT technique. In Section III, the proposed scheme is implemented in FIR filter realization. In Section IV, the proposed scheme is compared to the previously proposed ones. Finally, Section V, concludes this paper.

II. MCMAT Technique

Multiple constant Multiplication Accumulation Truncation (MCMAT) technique is more efficient to collect all the Partial Product(PPs) into a single Partial Product Bit(PPB) matrix with Carry Propagation Addition (CPA). It is needed to truncate the partial product bits to the required precision to reduce area cost. In this technique, a single row of PPBs is made undeletable (for the subsequent rounding), and the PPB elimination consists of only deletion and rounding [2].Instead of accumulating individual multiplication for each product, it is more efficient to collect all the PPs into a single PPB matrix to reduce the height of the matrix to two, followed by final carry propagation adder is shown in Fig.1.

2.1 Operations in MCMAT technique

The MCMAT truncated multiplier consists of several operations, including deletion, truncation, rounding, and final addition. In the first step, we perform the deletion that removes all the unnecessary PP bits that do not need to be generated is shown in Fig.1. a single row of PPBs is made undeletable (for the subsequent rounding), and the PPB elimination consists of only deletion and rounding. After the deletion of PP bits, we perform the per-column reduction and generate two rows of PP bits. After reduction, we perform the truncation that further removes the first row of n − 1 bits from column 1 to column n− 1.This step of truncation introduces truncation error.

After deletion, reduction, and truncation, the PP bits are added using a CPA to generate the final product of P bits. The bits in column 2 to column n−1can be safely removed before CPA because these bits are the only bits left in the columns after the deletion and truncation processes, and thus, they do not affect the carry bit to column n + 1 during the rounding process [2]. Before the final CPA, we add a bias constant of 1/2 ulp in order to achieve the round to nearest rounding with the rounding error. The bit at column n after the final CPA is also removed during the rounding process. Thus, the total error for the design of the MCMAT multiplier is bounded by the following equation

$$-ulp < E = (E_D+E_T+E_R) \leq ulp \qquad (2)$$

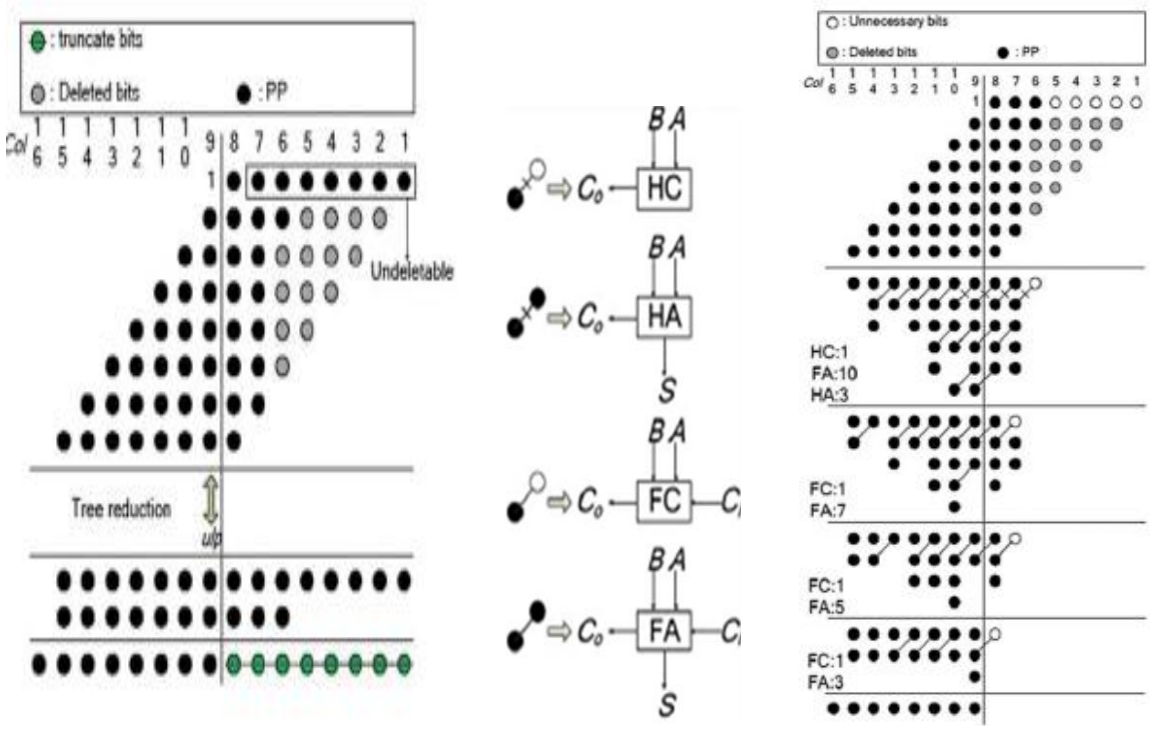

Fig.1.Truncated multiplier design using MCMAT technique

III. Proposed Work In Fir Filter Realization

Truncated multiplier can be effectively implemented in FIR filter structure. Conventional FIR filter performs ordinary multiplication of coefficient and input without considering the partial product bit length. Thus the structure can be made effective by replacing the existing multiplier with the proposed MCMAT truncated multiplier technique using Wallace Tree Compressor [4] for visible area reduction. Digital FIR filter implementation using MCMAT technique that removes unnecessary PPBs so that truncation error is not more than 1ulp, so the final result is precised.

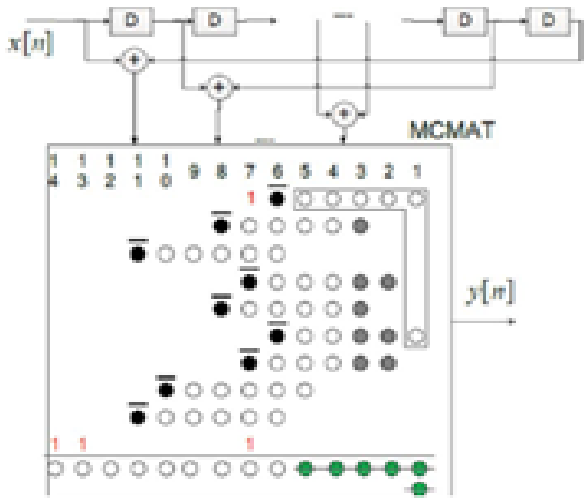

Fig.2. Digital FIR filter implementation using MCMAT technique

In Fig.2,the white circles in the L-shape block represent the undeletable PPBs. The deletion of the PPBs is represented by gray circles. After PP compression, the rounding of the resultant bits is denoted by crossed circles. The last row of the PPB matrix represents all the offset and bias constants required including the sign bit modifications. The proposed work of digital FIR filter design is implemented with MCMAT technique using Wallace tree compressor(5:2), where the results of the FIR filter structure shows the better area and power reduction compared to the conventional FIR filter.

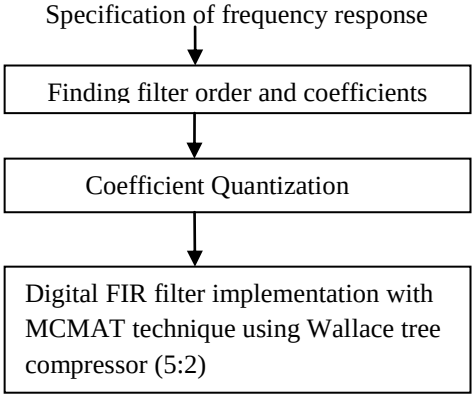

Fig.3. Digital FIR implementation with MCMAT technique using WTC

This modified FIR filter design and implementation can be divided into the following stages: Finding filter order and coefficients, coefficient quantization, digital FIR filter implementation with MCMAT technique using Wallace tree compressor is shown in Fig.3. In the first stage, the filter order and the corresponding coefficients are determined to satisfy the specification of the frequency response. Then, the coefficients are quantized to finite bit accuracy of 8 bits. The first two stages are implemented using MATLAB. Finally, optimization approaches such as MCMAT technique using WTC are used to minimize the area of hardware implementation.

IV. Results and Discussions

Multiplication plays a major role in FIR filter realization. The major aim of MCMAT technique is to provide high speed along with reduction in area. Area utilization and power utilization by the proposed method is less.

We implemented FIR filter with the low pass filter specification as given in Table I [7].M is the original filter order while EWL is the effective word length, f_{pass} and f_{stop} are the passband and stopband edge frequencies normalized to one, and A_{pass} and A_{stop} denote the corresponding peak to peak ripples.

TABLE I

Specification of the FIR filter under consideration

Filter	**M**	**EWL**	**f_{pass}**	**f_{stop}**	**A_{pass} (dB)**	**A_{stop} (dB)**
A(LP)	5	8	0.20	0.27	0.10	46

The MCMAT technique is simulated using MODELSIM and the output is shown in Fig.4. Here the inputs are given as a= 11111111 b=11111111 cf=11111111 d=11111111 e=11111111 f=11111111 g=11111111 h=11111111 k=11111111 l=11111111. For this input, outputs are produced as 11110110. For the given specifications, digital FIR filter implementation with MCMAT technique using WTC is simulated using MODELSIM and the output is shown in Fig.5.Here xn is the input,d1,d2,d3,d4 are the filter coefficients and y_n is the output.

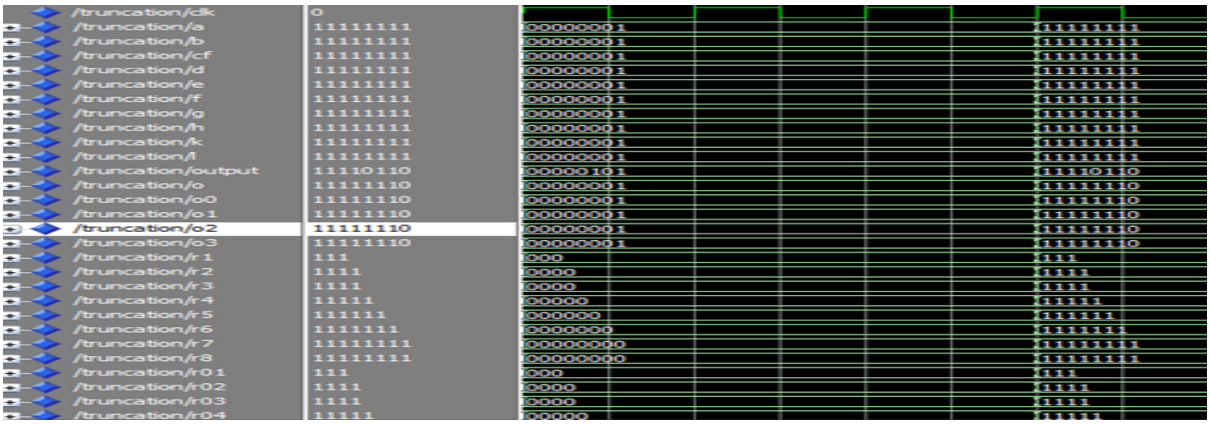

Fig.4. Simulation result of MCMAT technique

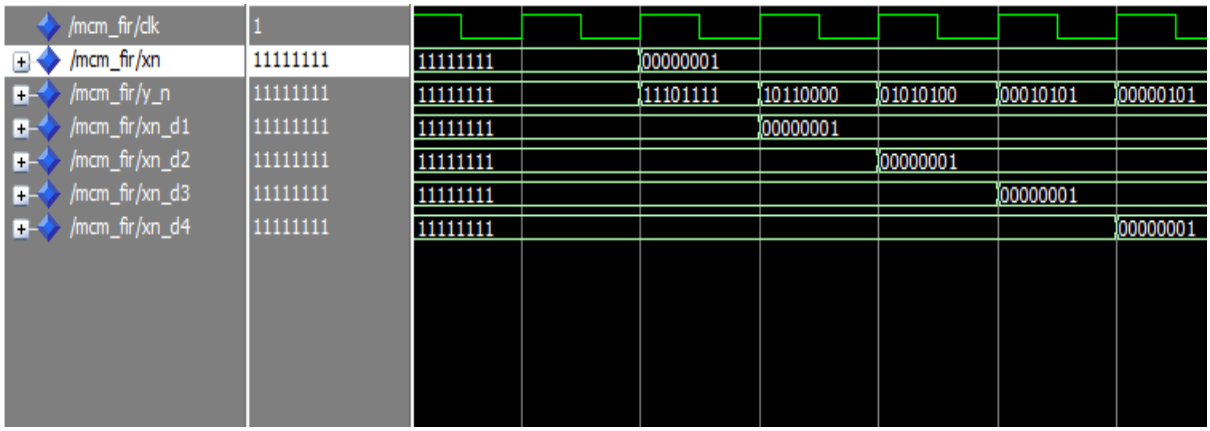

Fig.5. Simulation result of digital FIR implementation with MCMAT technique using WTC

The synthesis of the design is done using Xilinx ISE simulator and the implementation is done using Verilog HDL code. The synthesized report shows that the design in terms of area and speed is optimized. The comparison of area and power for the different architectures are given in the table below.

TABLE II
Synthesis results of Filter A with 5 tap LP

Parameters	Digital FIR filter design with MCMAT technique using CPA	Digital FIR filter design with MCMAT technique using WTC
Area (gate counts)	2,203	2,136
Power (mw)	55.57	47.62
No. of latches	229	149
No. of Slice registers	213	169

From the synthesized result as given in Table II, it is found that the proposed truncated multiplier technique using WTC consumes low area and low power compared to existing truncated multiplier technique using MCMAT technique for FIR filter realization.

After FIR filter coefficient multiplication operations, the output signals have larger bit width due to bit width expansion. In many practical situations, only partial bits of the full-precision outputs are needed. For this purpose, area efficient FIR filter is designed with MCMAT technique using WTC. The proposed design can effectively reduces the number of adders and the truncation error which is not more than 1 ulp. Hence the final output will be précised.

V. Conclusion

The proposed paper implements an area efficient low power FIR filter implementation. The area can be effectively reduced by the use of MCMAT technique for the filter coefficient multiplication with a slight reduction in speed. Thus the multiplication is carried out using WTC in place of Carry Propagation Addition(CPA). The MCMAT technique with WTC consists of lesser number of logic gates and as a result, it reduces the area of the design. The power is also reduced to the effectiveness of the design.

REFERENCES

[1] Charles. Roth Jr. ―Digital Systems Design using VHDL,Thomson Brooks/Cole, 7th reprint, 2005.
[2] H.-J. Ko and S.-F. Hsiao, "Design and application of faithfully rounded and truncated multipliers with combined deletion, reduction, truncation, and rounding," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 58, no. 5,pp. 304–308, May 2011.
[3] Soojin Kim and Kyeongsoon Cho , Design of High-speed Modified Booth Multipliers Operating at GHz Ranges, World Academy of Science, Engineering and Technology 37, 2010.
[4] Naveen Kr. Gahlan, Prabhat Shukla, Jasbir Kaur, "Implementation of Wallace Tree Multiplier Using Compressor", International journal on Computer Technology & Applications, vol. 3,pp. 1194-1199.Nov-Dec.2012.
[5] Y. J. Yu and Y. C. Lim, "Design of linear phase FIR filters in subexpression space using mixed integer linear programming," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 10, pp. 2330–2338, Oct. 2007.
[6] H. Samueli, "An improved search algorithm for the design of multiplierless FIR filters with powers-of-two coefficient," IEEE Trans. Circuits Syst., vol. 36, no. 7, pp. 1044–1047, Jul. 1989.
[7] Y. C. Lin and S. Parker, "Discrete coefficient FIR digital filter design based upon an LMS criteria," IEEE Trans. Circuits Syst., vol. 30, no. 10,pp. 723–739, Oct. 1983.