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New Topology for Transformer less Single Stage -Single Switch AC/DC Converter

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ABSTRACT : *This paper presents a transformer less single-stage single-switch ac/dc converter suitable for universal line applications (90–270 Vrms). The topology consists of a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is directly coupled to the output after the first power processing. With this direct power transfer and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus (less than 120 V) and low output voltage without a high step-down transformer. The absence of transformer reduces the size of the circuit , component counts and cost of the converter. Unlike most of the boost-type PFC cell, the main switch of the proposed converter only handles the peak inductor current of dc/dc cell rather than the superposition of both inductor currents. Tight voltage regulation is provided by using PID controller. Detailed analysis and design procedures and simulation of the proposed circuit are given .*

Keywords: *Direct power transfer (DPT), integrated buck– buck–boost converter (IBuBuBo), power-factor correction (PFC), single-stage (SS), transformer less.*

I. Introduction

The use of rectifiers in industrial applications started at the era of mercury converters with the electromechanical contact converter. DC machines are common in day to day use. But the supply that we get from power companies is AC. To use those machines AC supply has to be turned into DC supply by the use of a rectifier.The basic block diagram of AC/DC converter is shown in Figure 1.1. A rectifier is an electrical device that converts the incoming AC (alternating current) from a transformer or any other ac power source to pulsating DC (direct current). Rectifier may be made of diodes, solid states, vacuum tube, mercury arc valves and other components. Rectifiers are widely used in non linear loads which are connected with distribution systems which plays an important role in power system network (ex: UPS, discharge lamp, television, computer, fax machines, ferromagnetic devices, arc furnaces, energy savers etc).

The research on single-stage PFC ac/dc converters can be traced back to the early 1990s .Single-stage (ss) ac/dc converters have lot of applications because of its cost effectiveness, compact size, and simple control mechanism. Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell. Dc/dc cell is used for output voltage regulation . Several such methods are shown in references [1]–[7] .But their intermediate bus voltage is usually greater than the line input voltage and goes beyond 450 V at high-line application. Also there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. In addition, the other drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection[14] .

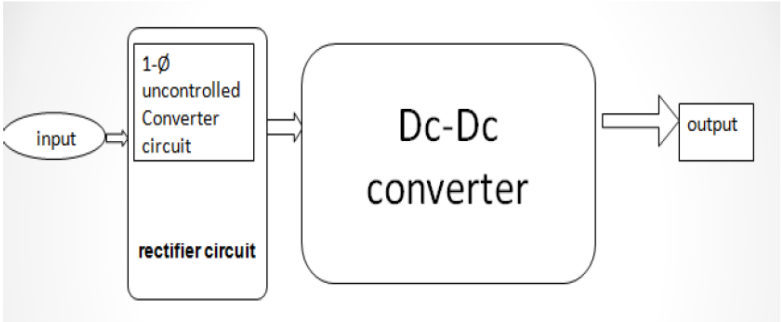


Figure1.1: Block Diagram Of AC/DC Converter

Some multistage power electronics system (e.g., in data center, electrochemical and petrochemical industries), the isolation has been done in the PFC stage, the second transformer in the dc/dc cell for the sake of isolation is considered as redundant. Hence, nonisolated ac/dc converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts[13]. For low voltage application (e.g.,≤48V), this high intermediate bus voltage increases components stresses on the dc/dc cell. This problem can be overcome by using a simple step-down dc/dc cell (i.e. buck or buck–boost converter).Extremely narrow duty cycle is needed for the conversion.This leads to poor circuit efficiency and limits the input voltage range for getting better performance.

Several methods were introduced to reduce the bus voltage much below the line input voltage during the years 2007-2011. Several such topologies have been reported in the references [9], [10], [13], [15]–[18]. Although the recently reported IBoBuBo converter in [13] is able to limit the bus voltage under 400 V, it cannot be applied to the low-voltage application directly due to the boost PFC cell. On the other hand, the converters in [9], [10], [15]–[18] employ different PFC cells to reduce the intermediate bus voltage. Among those converters in [9] and [15] use a transformer to achieve low output voltage either in PFC cell or dc/dc cell. Therefore, the leakage inductance is unavoidable. Converters in [10], [17], and [18], employ a buck–boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in references [18] and [10] process power at least twice resulting in low power efficiency. Moreover, the reported converters, in [16], and [17], consist of two active switches leading to more complicated gate control. Apart from reducing the intermediate bus voltage, the converter in [19] employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow, i.e., < 10%. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET.

To tackle the aforementioned problems, an intergrated buck–buck–boost (IBuBuBo) converter with low output voltage is proposed. This proposed circuit consists of a buck converter, used as PFC cell and a buck-boost converter as a dc/dc converter. This circuit is able to limit the bus voltage below the input voltage effectively.In addition, by In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. Therefore, a transformer is not needed to obtain the low output voltage. The converter is able to achieve:

1)low voltage stress on intermediate bus (less than 120 V) ;
2)high PF, compact size, Less cost;
3) low intermediate bus and output voltages in the absence of transformer;
4) simple control structure with a single-switch;
5) positive output voltage;
6) high conversion efficiency due to part of input power is processed once and
7) input surge current protection because of series connection of input source and switch.

II. Direct Power Transfer

In a conventional two-stage or S PFC ac/dc converter, there are two functional cells, i.e., PFC cell and dc/dc cell. AC input power is first transferred into somewhat pulsating dc power stored on intermediate bulk capacitors by the PFC cell. The stored dc power on the bulk capacitors is processed again by the dc/dc cell to the desired dc output power. So the input power is processed twice to reach the output, as shown in Fig. 2.1(a). Assuming the PFC cell has unity input power factor, and the efficiency of the PFC cell and dc/dc cell η_1 η_2 are and, respectively, we have output power

$$P_0 = P_{in}\eta_1\eta_2 \quad (1)$$

and the resultant efficiency of SS PFC ac/dc converter is

$$\eta = \eta_1\eta_2 \quad (2)$$

From the above equations, we can see that the dual power processing approach means lower conversion efficiency since it is the product of the efficiency of each power conversion

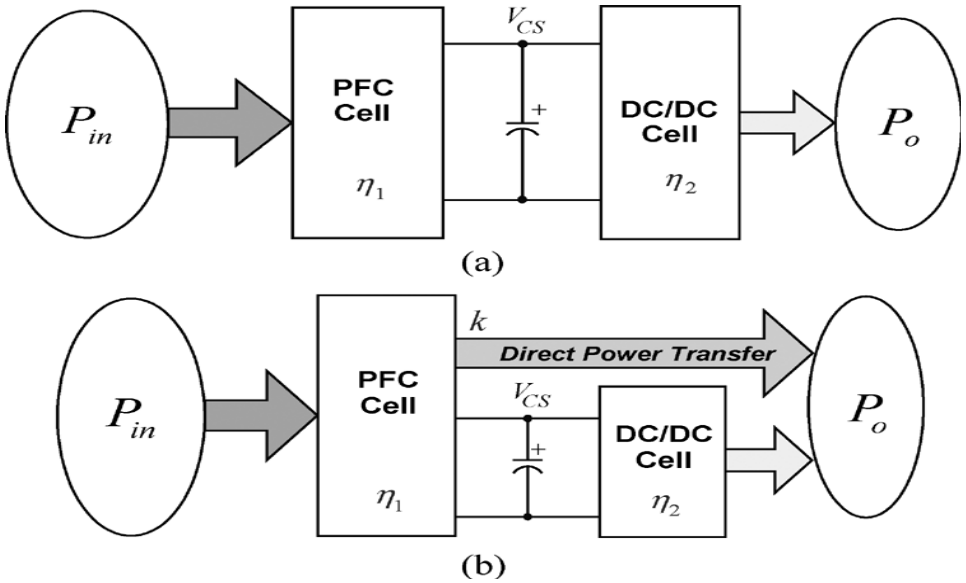


Figure. 2.1. Power transfer block diagrams of PFC ac/dc converters: (a) conventional power transfer and (b) proposed power transfer with DPT concept.

Direct power transfer approaches will allow a part of the input power to be processed only once and let the remaining input power to be processed twice while still achieving both high power factor and tight output

$$P_0 = P_{in}\eta_1 k + P_{in}\eta_1\eta_2(1-k) \quad (3)$$

regulation. Those power transfer approaches provide a new way to achieve more efficient and higher power rating PFC converters than the conventional double power processing approach. A block diagram of the proposed power transfer approach with the DPT concept is expressed in Fig. 2 .1(b). In Fig. 2.1(b), (1-k) portion of the power from the PFC cell is directly transferred to the output, and the remaining power from PFC cell is stored in the intermediate bus capacitor and then processed by the dc/dc cell. Based on this concept, we have so the efficiency of this S PFC ac/dc converter is

$$\eta = \eta_1\eta_2 + k\eta_1(1-\eta_2) \quad (4)$$

Comparing (2) with (4), it is clear that the converter with the DPT generally has higher efficiency than its counterpart without the DPT approach, simply because the converter with the DPT concept follows an inequality

$$\eta_1\eta_2 + k\eta_1(1-\eta_2) > \eta_1\eta_2 \quad (5)$$
$$where\_k < 1.\eta_1 < 1.and\eta_2 1.$$

The above efficiency comparison enhances our understanding why the DPT concept will help build an inherently more efficient PFC converter

III. Single-Stage PFC Converter

Power factor correction (PFC) techniques have become increasingly important since several regulations that are used to limit harmonic injection to the power utilities have been enacted recently. There are two basic PFC approaches, namely, active PFC and passive PFC. Active PFC, classified by the system configurations, can be categorized into two-stage and single-stage SS schemes. A two-stage scheme results in high power factor and fast response output voltage regulation by using two independent controllers and optimized power stages, as shown in Fig. 3.1(a). The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications.

An SS scheme combines the PFC cell and dc/dc power conversion cell into one stage, and typically uses only one controller and shares power switches, as shown in Fig. 3.1(b). It should be pointed out that from the viewpoint of functionality, in order to get high power factor and regulated output, an SS converter actually still needs to complete PFC and dc/dc regulating tasks as a two-stage converter. Usually, the high power factor of an SS PFC converter is guaranteed by operating the PFC cell in discontinuous current mode (DCM), while the fast response output regulation is achieved by the dc/dc cell. Although the single-stage scheme is especially

attractive in low cost and low power applications due to its simplified power stage and control circuit, major issues still exist, such as low efficiency and difficulty being moved to higher power level, and high as well as wide-range intermediate dc bus voltage stress.

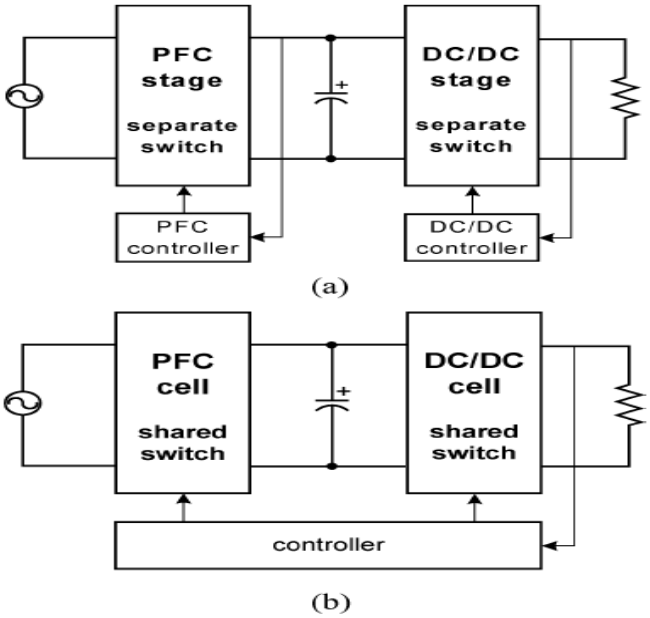


Figure. 3.1. Functional block diagram of PFC converters: (a) two-stage PFC converter and (b) typical single-stage PFC converter.

IV. Proposed Circuit and Its Operating Principle

The proposed I Bu Bu Bo converter, which consists of the merging of a buck PFC cell (L_1, S_1, D_1, C_O, C_B) and a buck–boost dc/dc cell ($L_2, S_2, D_2, D_3, C_O, C_B$) is illustrated in Fig. 4.1(a). Although L2 is on the return path of the buck PFC cell, does not contribute to the cell electrically. Thus, L2 is not considered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currentsin both inductors L1 and L2 at the beginning of each switching cycle t0 . Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

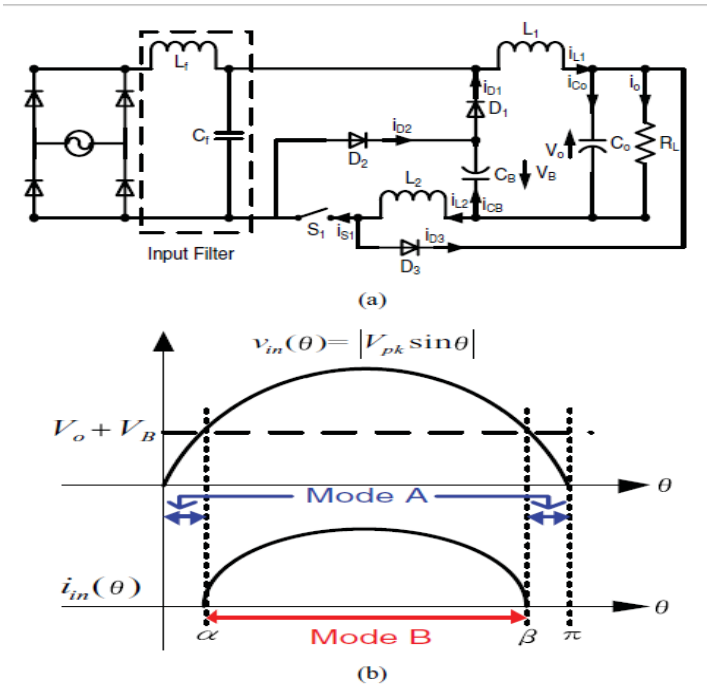


Figure 4.1: (a) Proposed IBuBuBo SS ac/dc converter. (b) Input voltage and current waveforms

ModeA(vin (θ)≤VB + Vo): When the input voltage vin (θ) is smaller than the sum of intermediate bus voltage VB , and output voltage Vo , the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage , owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 4.1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 4.2(a),(b), and (f). Fig. 4.3(a) shows its key current waveforms.

1) Stage 1 (period d1Ts in Fig. 4.3) [see Fig. 4.2(a)]: When switch S1 is turned ON, inductor L2 is charged linearly by the bus voltage VB while diode D2 is conducting. Output capacitor Co delivers power to the load.
2) Stage 2 (period d2Ts in Fig. 4.3) [see Fig. 4.2(b)]: When switch S1 is switched OFF, diode D3 becomes forward biased and energy stored in L2 is released to Co and the load.
3) Stage 3 (period d3Ts - d4Ts in Fig. 4.3) [see Fig. 4.2(f)]: The inductor current iL2 is totally discharged and only Co sustains the load current.

Mode B (vin (θ) > VB + Vo): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 4.2(c), (d), (e), and (f). The key waveforms are shown in Fig. 4.3(b).

1) Stage 1 (period d1Ts in Fig. 4.3) [see Fig. 4.2(c)]: When switch S1 is turned ON, both inductors L1 and L2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage (vin (θ) − VB − Vo), while diode D2 is conducting.
2) Stage 2 (period d2Ts in Fig. 4.3) [see Fig. 4.2(d)]: When switch S1 is switched OFF, inductor current iL1 decreases linearly to charge CB and Co through diode D1 as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in L2 is released to Co and the current is supplied to the load through diode D3. This stage ends once inductor L2 is fully discharged.
3) Stage 3 (period d3Ts in Fig. 4.3) [see Fig. 4.2(e)]: Inductor L1 continues to deliver current to Co and the load until its current reaches zero.
4) Stage 4 (period d4Ts in Fig.4.3) [see Fig. 4.2(f)]: Only Co delivers all the output power.

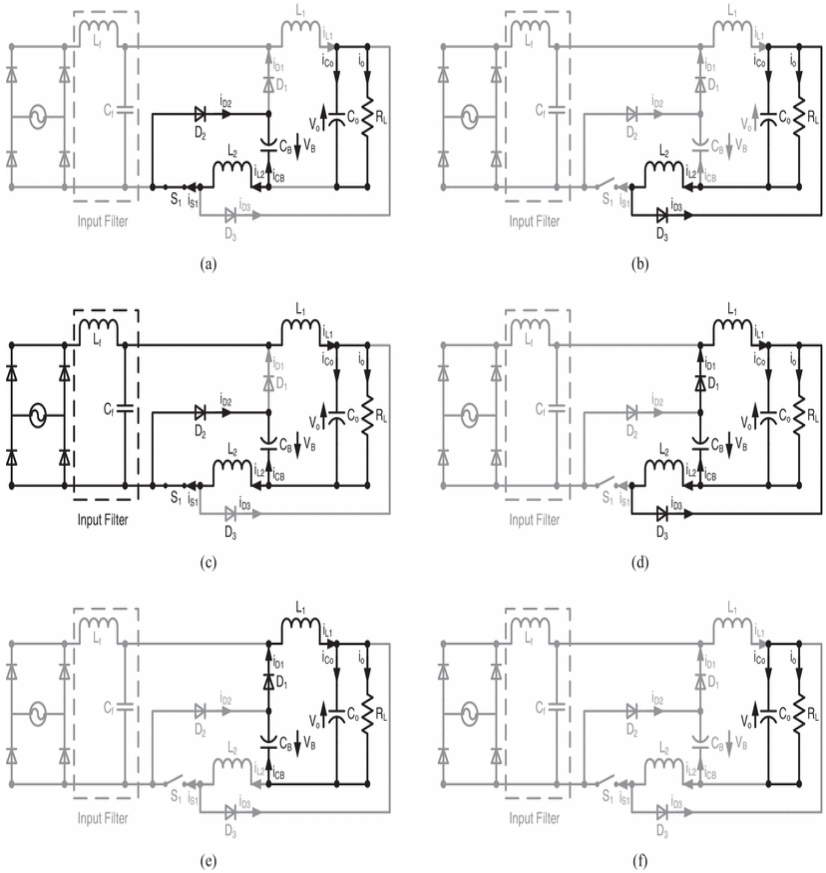


Figure. 4.2 Circuit operation stages of the proposed ac/dc converter.

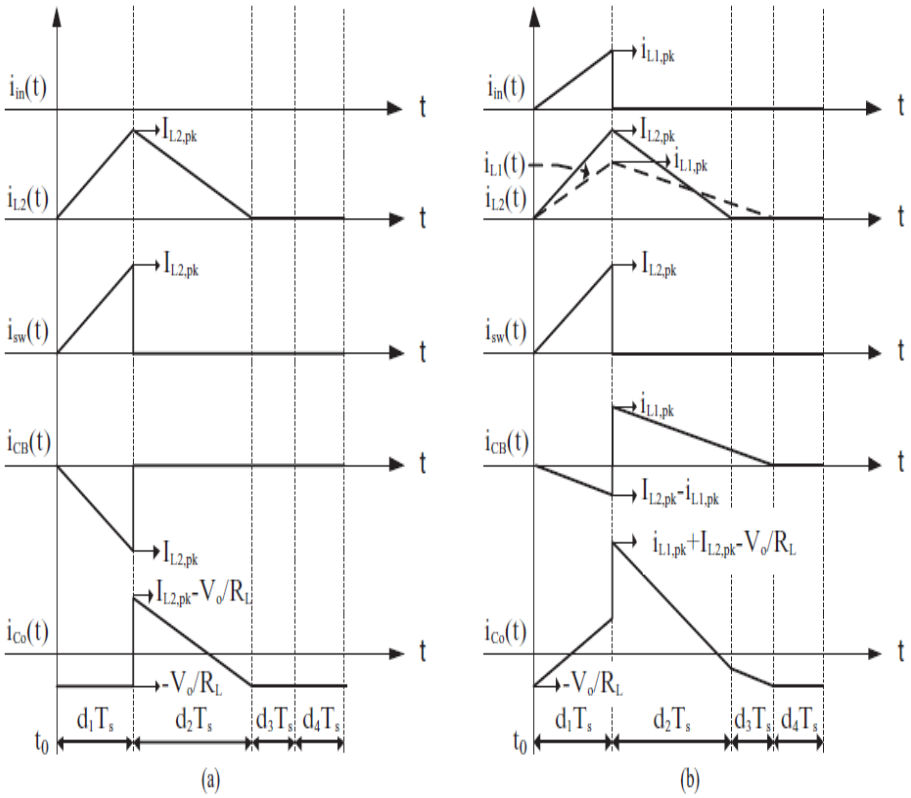


Figure. 4.3. Key waveforms of the proposed circuit

V. Design Consideration

To simplify the circuit analysis, some assumptions are made as follows:
1) all components are ideal;
2) line input source is pure sinusoidal, i.e. vin (θ) = Vpksin(θ) where Vpk and θ are denoted as its peak voltage and phase angle, respectively;
3) both capacitors CB and Co are sufficiently large such that they can be treated as constant DC voltage sources without any ripples;
4) the switching frequency fs is much higher than the line frequency such that the rectified line input voltage |vin (θ)| is constant within a switching period.

5.1. Circuit Characteristics

According to Fig.4.1 (b), there is no input current drawn from the source in Mode A, and the phase angles of the dead-time α and β can be expressed as

$$\alpha = \arcsin(\frac{V_T}{V_{pk}}) \tag{6}$$

$$\beta = \pi - \alpha = \pi - \arcsin(\frac{V_T}{V_{pk}}) \tag{7}$$

where VT is the sum of VB and Vo . Thus, the conduction angle of the converter is

$$\gamma = \beta - \alpha = \pi - 2\arcsin(\frac{V_T}{V_{pk}}) \tag{8}$$

From the key waveforms (see Fig. 4.3), the peak currents of the two inductors are:

$$i_{L1\_pk} = \begin{Bmatrix} \frac{v_{in}(\theta) - V_T}{L_1} d_1 T_S, \alpha < \theta < \beta \\ 0, otherwise \end{Bmatrix} \tag{10}$$

$$I_{L2\_pk} = \frac{V_B}{L_2} d_1 T_s \tag{11}$$

where Ts (1/fs) is a switching period of the converter. In (10) and (11), the dependency of iL1 pk on θ has been omitted for clarity. It is noted that L2 does not contribute in equation (10) even though it is on the current return path of the PFC cell.

In addition, by considering volt–second balance of the L1 and L2 , respectively, the important duty ratio relationships can be expressed as follows

$$d_2 + d_3 = \begin{Bmatrix} \frac{v_{in}(\theta) - V_T}{V_T} d_1, \alpha < \theta < \beta \\ 0, otherwise \end{Bmatrix} \tag{12}$$

$$d_2 = \frac{V_B}{V_O} d_1 \tag{13}$$

By applying charge balance of CB over a half-line period, the bus voltage VB can be determined. From Fig. 4.3, the average current of CB over a switching and half-line periods are expressed as follows:

$$\begin{aligned} < i_{CB} >_{sw} &= .5(i_{L1\_pk}(d_1 + d_2 + d_3) - I_{L2\_pk} d_1) \\ < i_{CB} >_{sw} &= d_1^{\,2} T_S \frac{[(v_{in}(\theta) - V_T) v_{in}(\theta)]}{L_1 V_T} - d_1^{\,2} T_S \left[\frac{V_B}{L_2}\right] \end{aligned} \tag{14}$$

And

$$\begin{aligned} < i_{CB} >_{\pi} &= \frac{1}{\pi} \int_0^{\pi} < i_{CB} >_{sw} d\theta \\ < i_{CB} >_{\pi} &= \frac{d_1^{\,2} T_S}{2\pi} \left[\frac{V_{pk}}{L_1} \left(\frac{V_{pk}}{V_T} \left(\frac{\gamma}{2} + \frac{A}{4} \right) - B \right) - \frac{\pi V_B}{L_2} \right] \end{aligned} \tag{15}$$

where the constants A and B are

$$\begin{aligned} A &= \sin(2\alpha) - \sin(2\beta) \\ B &= \cos(\alpha) - \cos(\beta) \end{aligned} \tag{16}$$

Putting equation (4.8) to zero due to the steady-state operation, this leads to

$$V_B = \frac{M V_{pk}^2}{2\pi (V_B + V_O)} \left[\pi - 2 \arcsin\left(\frac{V_B + V_O}{V_{pk}} \right) - \frac{2(V_B + V_O)\sqrt{(V_{pk} + V_B + V_O)(V_{pk} - V_B - V_O)}}{V_{pk}^2} \right] \tag{17}$$

where M is the inductance ratio L2/L1 .

As observed from equation(4.11), the bus voltage VB can be obtained easily by numerical method. It is noted that VB is independent on the load, but dependent on the inductance ratio M.. It is noted that the bus voltage is kept below 150 V at high-line input condition.

Similarly, the instantaneous and average input currents of the proposed circuit are

$$< i_{in} >_{sw} = \frac{i_{L1\_pk} d_1}{2} = \begin{Bmatrix} \frac{v_{in}(\theta) - V_T}{2L_1} d_1^{\,2} T_S, \alpha < \theta < \beta \\ 0, otherwise \end{Bmatrix} \tag{18}$$

And

$$\begin{aligned} I_{in} &= \frac{1}{\pi} \int_{\alpha}^{\beta} < i_{in} >_{sw} d\theta \\ I_{in} &= \frac{d_1^{\,2} T_S}{2\pi L_1} \left[V_{pk} B - \gamma V_T \right] \end{aligned} \tag{19}$$

Using equation (18) and (19), the rms value of the input current, average input power and power factor are given by

$$I_{in\_rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\beta}(< i_{in} >_{sw})^2 d\theta} \tag{20}$$

$$I_{in\_rms} = \frac{d_1^2 T_S}{2\sqrt{\pi L_1}}\sqrt{V_{pk}{}^2(\frac{\gamma}{2}+\frac{A}{4}) - 2V_{pk}V_T B + \gamma V_T{}^2}$$

$$P_{in} = \frac{1}{\pi}\int_{\alpha}^{\beta} v_{in}(\theta) < i_{in} >_{sw} d\theta \tag{21}$$

$$P_{in} = \frac{d_1^2 T_S V_{pk}}{2\pi L_1}\left[V_{pk}(\frac{\gamma}{2}+\frac{A}{4}) - V_T B\right]$$

$$PF = \frac{\frac{1}{\pi}\int_{\alpha}^{\beta} v_{in}(\theta) < i_{in} >_{sw} d\theta}{\frac{V_{pk}}{\sqrt{2}} I_{in\_rms}} \tag{22}$$

$$PF = \sqrt{\frac{2}{\pi}}\frac{V_{pk}(\frac{\gamma}{2}+\frac{A}{4}) - V_T B}{\sqrt{V_{pk}{}^2(\frac{\gamma}{2}+\frac{A}{4}) - 2V_{pk}V_T B + \gamma V_T{}^2}}$$

5.2 Condition for DCM

To ensure both cells working in DCM mode throughout the ac line period, we must determine their critical inductance first. To allow L1 working in DCM and from equation (12), we have the following inequalities

$$d_2 + d_3 \subseteq 1 - d_{1\_PFC} \tag{23}$$

$$d_{1\_PFC} <= \begin{Bmatrix} \frac{V_T}{v_{in}(\theta)}, \alpha < \theta < \beta \\ 0, otherwise \end{Bmatrix} \tag{24}$$

$$d_2 \subseteq 1 - d_{1\_DC/DC} \tag{25}$$

$$d_{1\_DC/DC} <= \frac{V_O}{V_O + V_B} = \frac{V_O}{V_T} \tag{26}$$

$$d_{1\_\max} = \begin{Bmatrix} \min(d_{1\_PFC}, d_{1\_DC/DC}), \alpha < \theta < \beta \\ d_{1\_DC/DC}, otherwise \end{Bmatrix} \tag{27}$$

$$R_{L\_\_\min} = \frac{V_O{}^2}{P_O} \tag{28}$$

where d1 PFC is the maximum d1 of the PFC cell.

By applying input–output power balance of the PFC cell and substituting in equation (27) into equation (21), the critical inductanceL1 crit is given by

$$L_{1\_crit} = \frac{R_{L\_\min} T_s V_{pk}}{2\pi V^2{}_0}\left[V_{pk}(\frac{\gamma}{2} + \frac{\sin(2\alpha) - \sin(2\beta)}{4}) + V_T(\cos(\beta) - \cos(\alpha))\right] d_{1\_\max}{}^2 \tag{29}$$

where RL min is denoted as the minimum load resistance of the converter.

For the dc/dc cell sustaining all the power to the load under DCM operation in Mode A, the critical inductance L2 crit is the smallest. Under the input–output power balance of the dc/dc cell, the critical inductance L2 crit can be determined. The input power of the dc/dc cell in Mode A is given by

$$P_{in\_DC/DC} = \frac{V_B}{\pi}\int < i_{DC/DC} >_{sw} d\theta = \frac{V_B{}^2 T_S d_1^2}{2L_2} \tag{30}$$

where < idc/dc >sw is the instantaneous input current of dc/dc cell. Hence, by substituting (27) into (30), the critical inductance L2 crit is given by

$$L_{2\_crit} = \frac{R_{L\_\min} V_B{}^2 T_S}{2V^2{}_0} d^2{}_{1\_\max} \tag{31}$$

4.3. Capacitors Optimization

To determine the size of the intermediate bus capacitor CB , we can consider the hold-up time (thold up) of the circuit. The bus capacitor CB will sustain all the output power within t_hold up when the ac input source is removed. In normal practice, the hold-up time is one of the ac line cycle. In addition, the maximum capacitance of CB to meet this hold-up time requirement is determined under the low-line and full output load conditions. Thus, the size of CB is expressed as follows:

$$C_B = \frac{2P_O t_{hold\_up}}{V^2{}_{B\_nominal} - V^2_{B\_\min}} \tag{32}$$

where hold up time is:

$$t_{hold\_up} = \frac{\alpha}{\omega} = \arcsin\left(\frac{V_B + V_O}{V_{pk}}\right) \tag{33}$$

Apart from the size of CB, it is noted that the line frequency ripple on the output capacitor Co is inevitable since a portion of the input power is coupled to the load directly. However, this ripple can be reduced by increasing its capacitance.

VI. Design of the Simulation Prototype

The performance of the proposed circuit is verified by using MATLAB/ Simulink. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage (< 150V) and high power factor (> 96%), the inductance ratio has to be optimized. The lower the bus voltage of the converter, the lower voltage rating capacitor (150 V) can be used.

6.1 Specifications

1) output power: 100 W;
2) output voltage: 19 Vdc
3) power factor: > 96%;
4) intermediate bus voltage: < 150V;
5) line input voltage: 90–270 Vrms/50 Hz;
6) switching frequency (fs): 20 kHz.
7) M =.4

6.2 Input filter

A low-pass filter is a filter that passes low-frequency signals and attenuates (reduces the amplitude of) signals with frequencies higher than the cutoff frequency. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass. Low-pass filters exist in many different forms, including electronic circuits (such as a hiss filter used in audio), anti-aliasing filters for conditioning signals prior to analog-to-digital conversion, digital filters for smoothing sets of data, acoustic barriers, blurring of images, and so on. The moving average operation used in fields such as finance is a particular kind of low-pass filter, and can be analyzed with the same signal processing techniques as are used for other low-pass filters. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the longer-term trend.

F_r as the resonance frequency

$$F_r = 1/(2\pi\sqrt{L_f C_f}) \tag{34}$$

Assume the value of L_f and find C_f

Here we take F_r as 2500 Hz assume L_r as 2mH then, = 2µF

6.3 Intermediate bus voltage

Equation (17) is solved by using MATLAB.

```
m=.4;
vpk= 230*sqrt(2);
vo=19;
f=vb-(((m*vpk*vpk)/(2*pi*(vb+vo)))*((pi(2*asin((vb+vo)/vpk)))-(2*(vb+vo)*sqrt((vpk+vb+vo)*(vpk-vb-
vo))/(vpk*vpk))));
df = diff (f);
vb=1;
for    M=1:10
p=eval(f);
q=eval(df);
eval('vb=vb-(p/q)');
end
```

For input given is 230V ,intermediate voltage VB obtained is 98.73V.

It is noted that VB is independent on the load, but dependent on the inductance ratio M. Depicts the relationship among VB , rms value of the line voltage, and inductance ratio M. It is noted that the bus voltage is kept below 150 V at high-line input condition.

Table 2:different intermediate voltage as input varies

INPUT VOLTAGE	INTERMEDIATE VOLTAGE
90V	32V
230V	98.7V
270V	117.8V

6.4 Intermediate capacitor

$Let,$

$P_O = 100W, V_{B\_nominal} = 98.7V, ripple = 40\%V_O, V_{B\_\min} = 98.5V, V_O = 19V$

$then,$

$V_{pk} = 230 * \sqrt{2}V = 325.26V$

$\alpha = .370 radians$

$\beta = 2.77 radians$

$\gamma = 2.40 radians$

$\omega = 2 * \pi * f = 314.15 radians/\sec$

Using equation (33)

t_holdup =1.17ms

Assume ripple of about 40% of the output voltage

Using equation (32) intermediate capacitor is:

CB = 5mF

6.5 Buck and buck- boost inductor

Using equation (24) and (26)

$$d_{1\_PFC} = \begin{Bmatrix} .362, \alpha < \theta < \beta \\ 0, otherwise \end{Bmatrix}$$

$$d_{1\_DC/DC} <= \frac{V_O}{V_O + V_B} = \frac{V_O}{V_T} = .161$$

Using equation (27) d_max is choose as

$$d_{1\_\max} = \begin{Bmatrix} .161, \alpha < \theta < \beta \\ .161, otherwise \end{Bmatrix}$$

$$R_{L\_\_\min} = \frac{V_O{}^2}{P_O} = 3.61\Omega$$

where RL min is denoted as the minimum load resistance of the converter.

$$Let,$$
$$V_O = 19V$$
$$V_{pk} = 230 * \sqrt{2}V = 325.26V$$
$$\alpha = .370 radians$$
$$\beta = 2.77 radians$$
$$\gamma = 2.40 radians$$

Using equation (29) and (31)

$$L_{1\_crit} = 188\mu H$$
$$L_{2\_crit} = 63\mu H$$

6.6 Output capacitor filter

Output capacitor is used to eliminate the ripple in output voltage

$$C_O = \frac{1}{4fR_L}(1 + \frac{1}{\sqrt{2}R.F}) \qquad (35)$$

$$R.F = \frac{V_{ac}}{V_{dc}} = .27$$
$$C_O = 5mF$$

Table 3 circuit components

PARAMETERS	VALUES
Input Filter Inductor	2 mH
Input Filter Capacitor	2 µF
Inductor L1	188µH
Inductor L2	63µH
Capacitor CB	5mF
Capacitor CO	5mF

VII. Simulation and Results

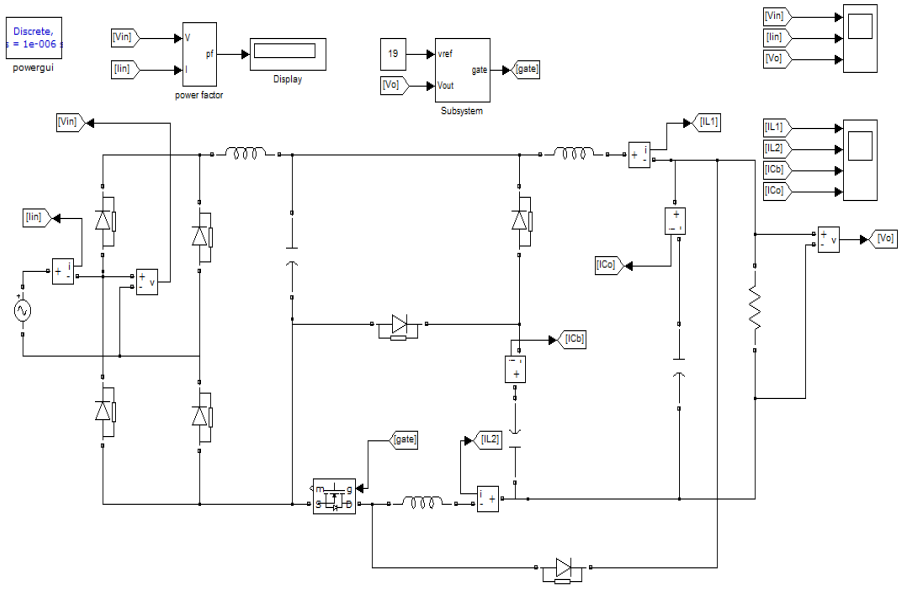
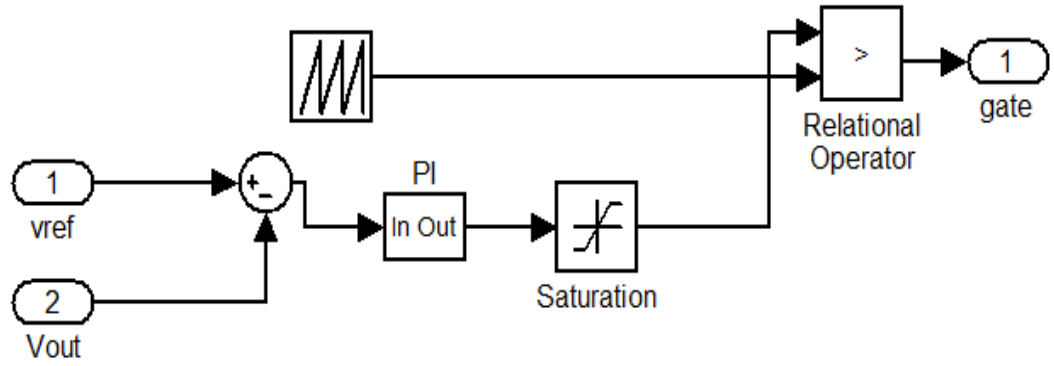


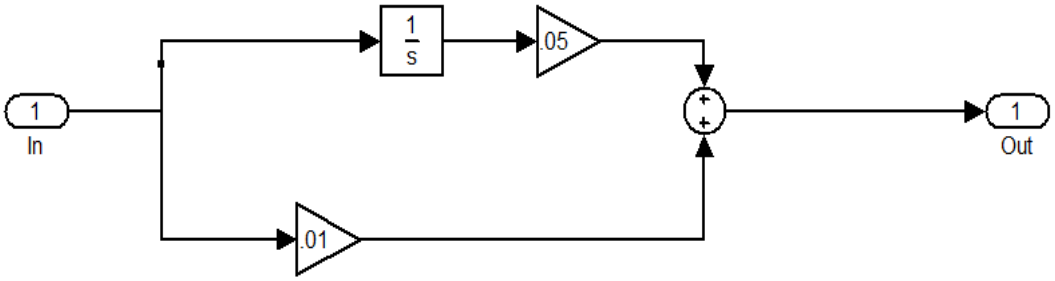
Fig 6.1: Proposed Circuit In MATLAB/Simulink

7.1 Subsystems

a) Pulse generating system



b) PI Controller



c) PF measurement

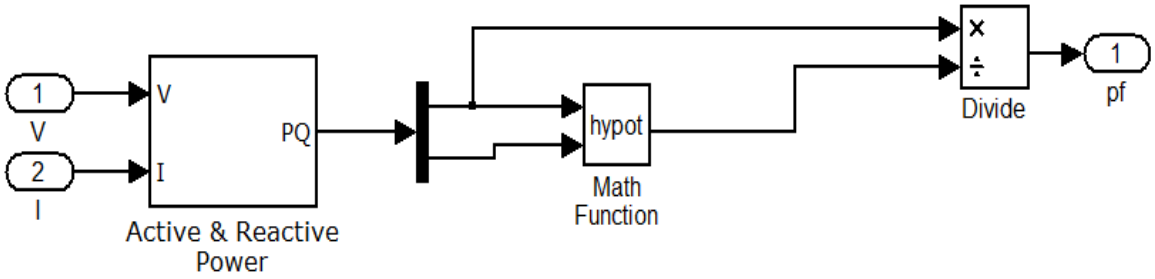


Fig 6.2 Different Subsystems used in Simulation

7.2 Results

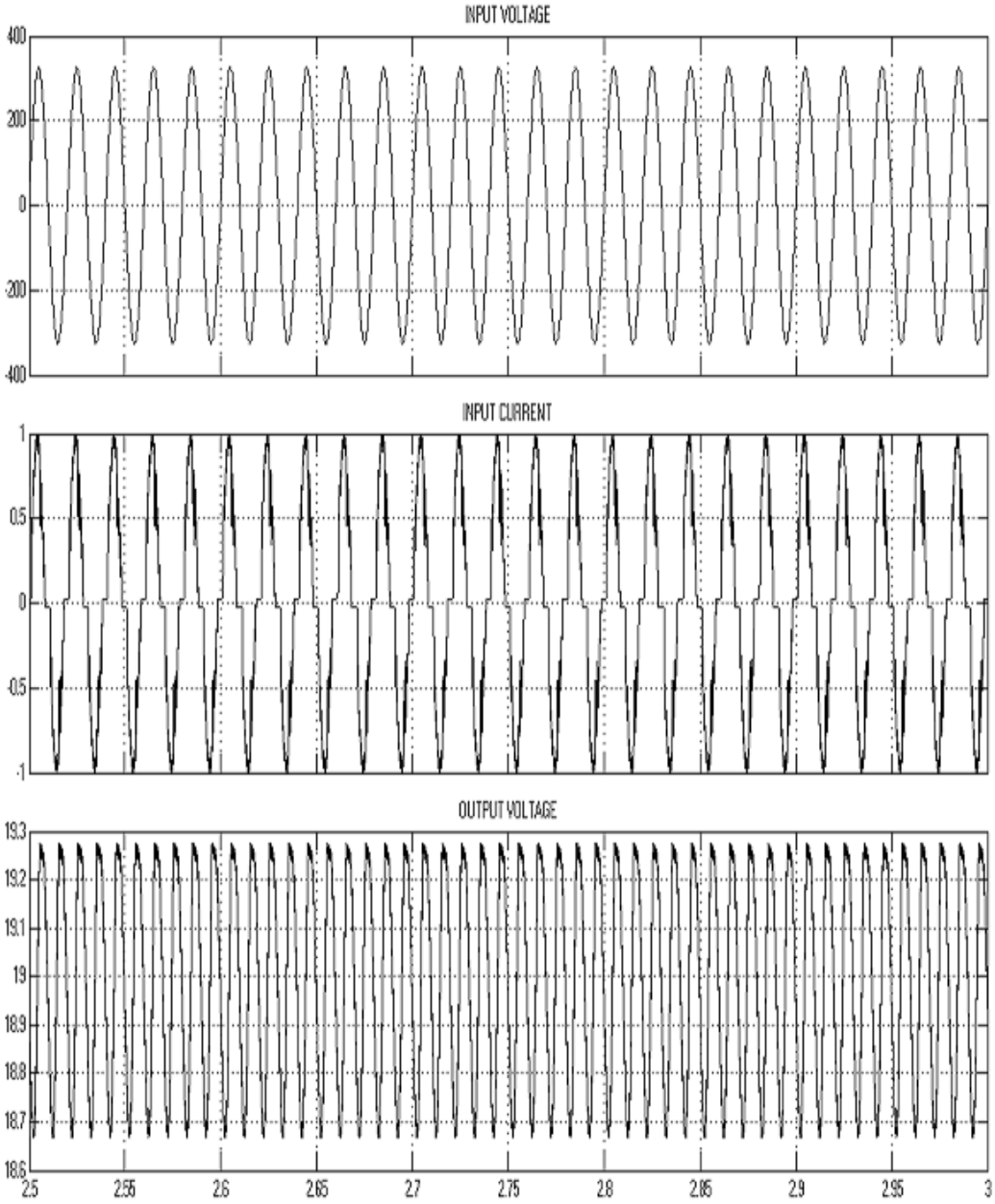


Fig 6.3 waveforms of input voltage, input current,output voltage

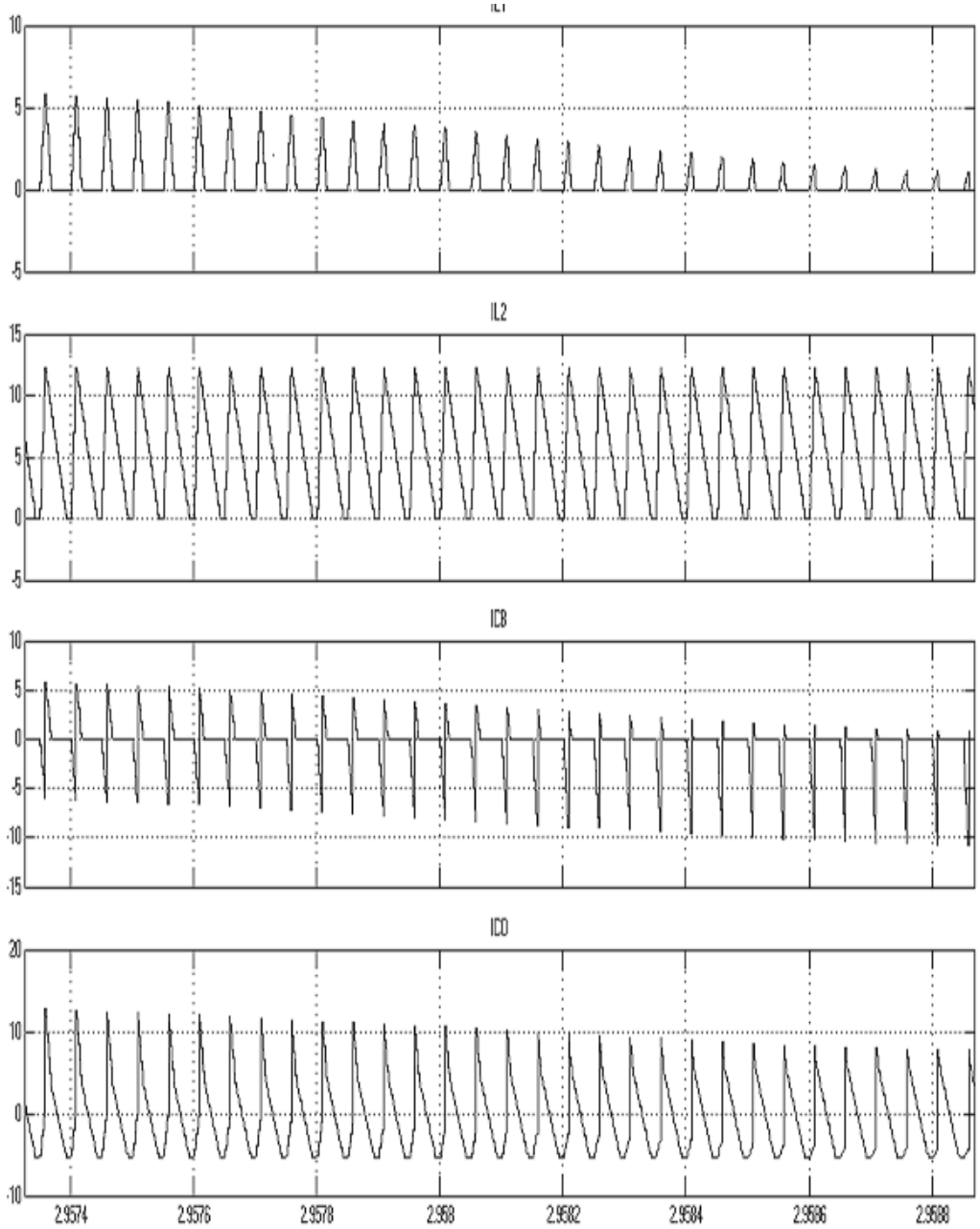


Fig 7.4: Waveforms of IL1, IL2, ICB, ICO

VIII. Conclusion

The proposed AC/DC converter has been simulated, and the waveforms have been observed. The intermediate bus voltage of the circuit is able to keep low at all input and output conditions and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. Moreover, the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of transformer, the demagnetizing circuit, the associated circuit dealing with leakage inductance and the cost of the proposed circuit are reduced compared with the isolated counterparts. Because of the direct power transfer path in the proposed converter, it is able to achieve high efficiency.

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