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A DC-DC Converter with Ripple Current Cancellation Based On Duty Cycle Selection

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Abstract: *In this paper a boost dc-dc converter is proposed based on the concept of ripple current cancellation. This proposed system has the novel capability of cancelling the input current ripple at an arbitrarily preselected duty cycle. This is accomplished without increasing the count of the number of components in contrast to other solutions available in the conventional system. In addition to this, the converter also features a high voltage gain without utilizing extreme values of duty cycle or boosting transformers. These features make the converter ideal to process electric power coming from low-voltage power-generating sources, such as renewables. This system also provides details on the principle of operation via topological considerations and a mathematical model. The key factor of reactive component sizing is also discussed in detail. The proposed boost dc-dc converter is evaluated by simulating in MATLAB/Simulink software.*

Keywords: *Boost converter, Complete charge interchange (CCI), Current ripple cancellation, Duty Cycle Selection, Switched capacitor (SC).*

I. Introduction

Dc – Dc converters are widely used in today's industrial or commercial electronic devices to manipulate a dc voltage source. As the name implies, dc – dc converters work exclusively to take a dc voltage input and convert it to output at a different level of dc voltage. They can either step-up or step-down the input dc voltage while maintaining minimal power loss during the process. There are many different topologies available for use such as Buck (step down), Boost (Step up), Fly back, Push-Pull, etc. This versatility is the reason that dc – dc converters are popular among many current electronic devices.

Owing to worldwide energy crisis and awareness of environmental protection in recent years, to seek for substitute energy has become an important issue. Among many substitute energies, solar energy, wind energy, hydroelectric power, biomass energy, and fuel cells are green energies with potential development.

A fuel Cell is a device that converts the chemical energy from a fuel into electricity through a chemical reaction with oxygen or another oxidizing agent. The fuel cell is one of the most promising power supplies and is drawing attention by many researchers. Due to high efficiency, high stability, low energy consumed and friendly to environment, this technology is in the progress to commercialize. Fuel cell has higher energy storage capability thus enhancing the range of operation for automobile. It is a source of clean energy, only water is produced after the reaction; hence, there is hardly any environmental pollution. Fuel cells as a source of power are usually applied to electric hybrid automobiles, distributed electric generation system, and portable and stationary power. In order to link the low output voltages of the fuel cells to an inverter or a load boost-type architecture with a large voltage gain is required.

The major challenge of designing a boost converter for high power application is how to handle the high current at the input and high voltage at the output. Another important requirement for a converter in renewable energy applications (for example, in fuel cells) is to drain a continuous current with minimum ripple. In boost converter designs, the input current-ripple is required to be a small percentage of the input dc current. It is well known that the current ripple is smaller as the input inductor becomes larger. This is a constraint since increasing the input inductor increases the size and cost of the converter. Several solutions have been proposed for addressing this drawback of the boost converter. In addition, a large inductor also slows down the open loop transient response of the converter. Therefore, converters combining these two features are expected to find many applications within the renewable-energy context.

Here, a boost converter topology is presented which combines two principles highly used in state of-the-art power converters:

- At the converter's input, two inductors are connected for canceling the input current ripple, and

- At the converter's output, an SC voltage multiplier is utilized to increase the voltage gain.

The SC stage has been improved by using a small resonant inductor to limit the peak current resulting from the switching process and hence preventing large current spikes. The presented converter does not require transformers or coupled inductors and is intended to be used along with fast-switching power semiconductors. Also, the topology presented herein is able to cancel the input current ripple. Furthermore, it combines a complete charge interchange- switched capacitor (CCI-SC) circuit with a boost converter into a single converter.

II. Literature Survey

In high voltage multilevel boost converter the leakage resistance in the inductor-charging loop limits the boost ratio. Because of this, a boost converter is not used when the required boost ratio is higher than four. A standard approach to overcome this issue is the use of small reactive components by increasing the converter's switching frequency for a given amount of acceptable ripple. In three switch and high voltage dc-dc converters, small reactive elements also feature a small leakage resistance. However, the finite switching time in actual power semiconductors limits the switching frequency when the duty ratio is too small or too high. A traditional solution to this is the employment of intermediate transformers to increase the voltage without using extreme values of duty cycles.

Several topologies have been proposed for overcoming the above challenges, including the use of coupled inductor and/or transformers. Moreover, the literature offers additional solutions based on the switched capacitor (SC) principle, with a combination of converters featuring coupled inductors with voltage multipliers or SC multipliers. Converters without coupled inductors based on pure SC circuits have found applications in low-power on-chip applications, but at larger power levels, solutions based on traditional converters have been preferred due to the number power semiconductors required, current spikes among capacitors, and high switching frequency limitations.

The interleaving of SC circuits has also been proposed as a solution for high voltage gain in switched capacitor based converters that already exist. A number of power converters for higher power application that eliminate the use of coupled inductors or transformers have been also proposed literatures. These topologies are expected to penetrate the market of high-gain dc–dc converter as silicon carbide and other wide-band gap fast-switching power semiconductors become available. This will make the switching frequency limitation in power converters to become a transformer issue, since transformers increase their losses when the frequency is too high.

In the paper of Gu et al. , of large gain hybrid dc-dc converter they use the SC principle with complete charge interchange (CCI) along with an additional pulse width modulated (PWM) boost converter for voltage regulation. As explained in the literature SC based resonant converter SC circuits with CCI are not utilized for voltage regulation, because this negatively affects the converter's efficiency. However, combining a CCI-SC circuit with a PWM controlled converter allows for optimizing the efficiency of both converters. In summary, converters with a high voltage gain which do not require a transformer, coupled inductors, or extreme duty cycle values are highly desirable given the quick penetration of low-voltage power-generating sources.

Different from coupled inductor based converters, the proposed converter does not require transformers or coupled inductors and is intended to be used along with fast-switching power semiconductors. Different from hybrid SC converter, the topology proposed herein is able to cancel the input current ripple. Furthermore, it combines a CCI-SC circuit with a boost converter into a single converter and is able to provide voltage regulation without sacrificing the converter's efficiency.

III. Presented Converter Topology

3.1 Novel Boost Converter Topology

The improved boost converter topology is shown in Figure 3.1 As the figure suggests, the topology contains two transistors (S_1 and S_2), three diodes (d_1, d_2, and d_3), three capacitors (C_1, C_2, and C_3), two inductors for energy storage (L_1 and L_2), and a small inductor (L_3) for current limiting through d_3. In practical implementation, L_3 is around 100 times smaller than L_2 and 50 times smaller than L_1. As a result of its reduced size, small-ripple approximations do not apply to $L3$, and hence, the selection of its inductance is based on the CCI between C_2 and C_3.

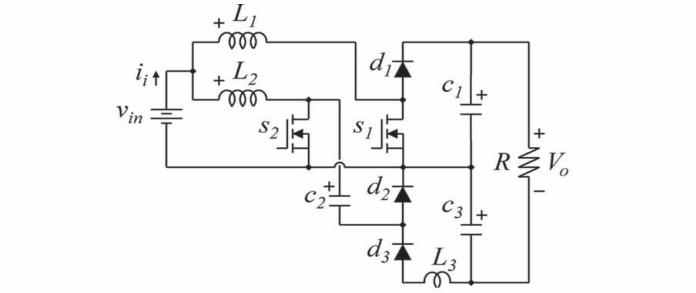


Figure 3.1: Circuit Schematic of the new topology

The transistors switch complementarily, i.e., when S_1 is closed, S_2 is open and vice versa. The operation of the converter may be explained considering the small-ripple approximation for the voltage across capacitors and continuous conduction mode for L_1 and L_2. The details on the circuit operation are conveniently introduced by employing several analytical waveforms. As shown in Figure 3.2 and 3.3, the converter has two equivalent circuits resulting from the switch action. When S_1 is on (and S_2 is off), the topology is represented by the equivalent circuit in Figure 3.2. During this time, the diode d_1 is reversely biased, blocking the voltage across C_1. Similarly, diode d_3 is reversely biased, blocking the voltage across C_3. The current through L_2 forces the diode d_2 to be closed since transistor S_2 is open.

The typical waveforms for the currents through L_1 and L_2, the input current, and the switching sequence for S_1 and S_2 are shown in Figure 3.4 from top to bottom. While S_1 is conducting, the current through L_1 rises with a slope of v_{in}/L_1, and L_2 discharges at a rate of $(v_{in} - v_{C2})/L_2$. biased, blocking the voltage across C_3. The current through L_2 forces the diode d_2 to be closed since transistor S_2 is open.

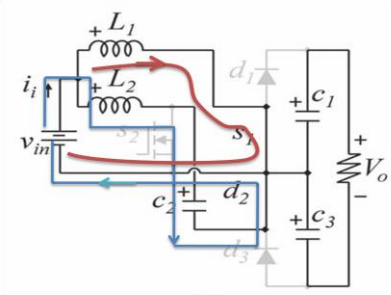


Figure 3.2: Equivalent circuit when S_1 is on

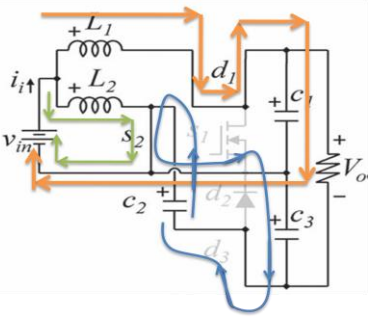


Figure 3.3: Equivalent circuit when S_2 is on

The typical waveforms for the currents through L_1 and L_2, the input current, and the switching sequence for S_1 and S_2 are shown in Figure 3.4 from top to bottom. While S_1 is conducting, the current through L_1 rises with a slope of v_{in}/L_1, and L_2 discharges at a rate of $(v_{in} - v_{C2})/L_2$.

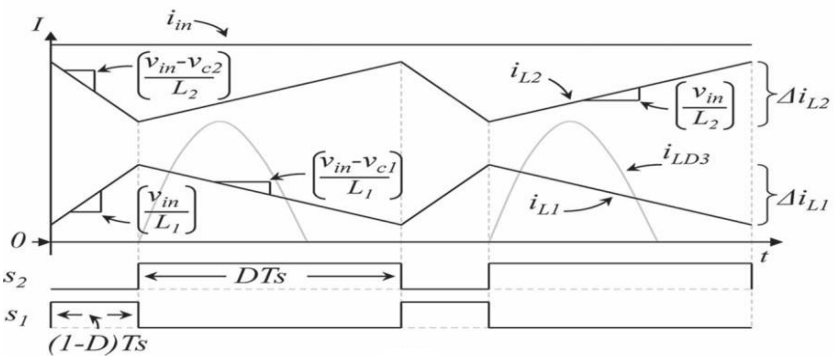


Figure 3.4: Waveforms of input current, current through input inductors,and switching sequence

On the other hand, while S_2 is on (and S_1 is off), the resulting equivalent circuit is as shown in Figure 3.3. During this time, the L_1 discharges with a slope that is equal to $(v_{in}-v_{C1})/L_1$, while L_2 charges at a rate of v_{in}/L_2. Furthermore, while S_2 is conducting, the capacitors C_2 and C_3 are connected in parallel, leading to an SC-type behavior. As a result of this, a small inductor (L_3) is needed in order to limit the peak current around this loop.

A typical waveform for the current through L_3 is also shown in Figure 3.4. A key feature of the boost converter topology can be observed in Figure 3.1 that is the converter's input current corresponds to the sum of the currents through L_1 and L_2. Since L_1 and L_2 charge/discharge in a complementary manner, one can size those two inductors such that the input current is ripple free for a selected value of the converter's duty cycle. The current waveforms shown in Figure 3.4 correspond to a converter that features a zero input current ripple at a duty cycle of *D* = 75%. This is possible if both inductors are charged with the same voltage and $L_2 = 3L_1$.

3.2 Principle of Switched Capacitor

A switched capacitor is an electronic circuit element used for discrete time signal processing. It works by moving charges into and out of capacitors when switches are opened and closed. Usually, non-overlapping signals are used to control the switches, so that not all switches are closed simultaneously.

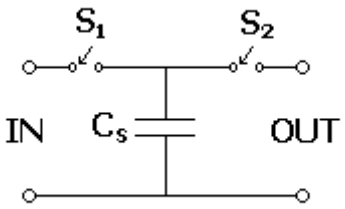


Figure 3.5: Circuit schematic of switched capacitor

The simplest switched capacitor (SC) circuit is the switched capacitor resistor, made of one capacitor C and two switches S_1 and S_2 which connect the capacitor with a given frequency alternately to the input and output of the SC. Each switching cycle transfers a charge q from the input to the output at the switching frequency f

IV. Analysis and Selection of Components

The architecture corresponds to an interleaving-type converter, combining features from a boost converter and a high-voltage converter. The topology features a small inductor for peak current limiting which has no effect on the basic operation of the converter for power transfer. In addition, the interleaving of two inductors allows current ripple cancelation at an arbitrary preselected duty cycle. Furthermore, as there are only two switches, the converter is controlled by a single duty cycle.

4.1 Voltage Gain Analysis

The dynamics of L_1, L_2, and C_1 may be conveniently analyzed considering their average behavior, as their state variables feature triangular waveforms similar to those in traditional dc/dc converters. On the other hand, C_2, C_3, and L_3 form a SC circuit, and therefore, their dynamic behavior has to be formulated with additional considerations. However, a number of the converter's features can be explained focusing on L_1, L_2, and C_1, where dynamic averaging applies. Under this assumption, switching functions may be readily replaced by their corresponding duty cycles. For the analysis hereinafter, the converter's duty ratio *d*(*t*) is defined as percentage of time over the switching period that the switch S_2 is on, i.e.,

$$d(t) = \frac{1}{T_s}\int_t^{t+T_s} q_2(\tau)d\tau \qquad (1)$$

Where T_S is the switching period and q_2 is the switching function of S_2 that is equal to one while S_2 is closed and zero otherwise. Under this assumption, and neglecting for now the inductors' equivalent series resistance (ESR), the equations that represent the average dynamics for inductors L_1 and L_2 are

$$L_1 \frac{di_{L1}}{dt} = d(v_{in} - v_{c1}) + (1-d)v_{in} \quad (2)$$

$$L_2 \frac{di_{L2}}{dt} = d(v_{in}) + (1-d)(v_{in} - v_{c2}) \quad (3)$$

In steady state, the average voltage across the inductors must be equal to zero. Thus, by zeroing the left-hand side of equations (1) and (2), the steady state voltage across C_1 and C_2 may be expressed as

$$V_{C1} = \frac{1}{D} V_{in} \quad (4)$$

$$V_{C2} = \frac{1}{1-D} V_{in} \quad (5)$$

In equations (4) and (5), capital letters denote steady-state quantities. It readily follows from equations (4) and (5) that the voltages across C_1 and C_2 are proportional to one another, i.e.

$$V_{C1} = \frac{1-D}{D} V_{C2} \quad (6)$$

$$V_{C2} = \frac{D}{1-D} V_{C1} \quad (7)$$

On the other hand, the equation that represents the average dynamics for C_1 is

$$C_1 \frac{dv_{C1}}{dt} = di_{L1} - \frac{v_{C1}+v_{C3}}{R} \quad (8)$$

In steady state, the average current through C_1 must be equal to zero, which leads to the following expressions for the current through L_1

$$I_{L1} = \frac{1}{D}\left(\frac{V_{C1}+V_{C3}}{R}\right) \quad (9)$$

As C_2 and C_3 form an SC circuit, average dynamic equations do not apply. However, the steady-state current through L_2 can be computed by input/output power balance considerations. It becomes

$$I_{L2} = \frac{1}{1-D}\left(\frac{V_{C1}+V_{C3}}{R}\right) \quad (10)$$

Furthermore, from figure 3.1, the output voltage is

$$V_O = V_{C1} + V_{C2} \quad (11)$$

Thus combining equations (4), (5) and (9)-(11), the converter voltage gain becomes

$$\frac{V_0}{V_{in}} = \frac{1}{D(1-D)} \quad (12)$$

The improved circuit has an SC stage which maybe increased by including additional capacitors and diodes Capacitors C_2 and C_3 work in an SC way because C_2 clamps the voltage across C_3 while the switch S_2 is closed. This is because the energy stored in L_3 is negligible compared to other energy storage elements in the converter. Furthermore, in steady state, C_2 and C_3 feature the same average voltage.

$$V_{C2} = V_{C3} \quad (13)$$

The gain expressed by equation (12) corresponds to an ideal case as the inductor's ESR has been neglected. In a practical implementation, the leakage resistance in inductors greatly limits this gain. In order to quantify this, consider first rewriting equations (9) and (10) using (6) and (7) and (11).

$$I_{L1} = \left(1 + \frac{D}{1-D}\right)\frac{1}{D}\frac{V_{C1}}{R} = \frac{1}{D(1-D)}\frac{V_{C1}}{R} \quad (14)$$

$$I_{L2} = \left(1 + \frac{1-D}{D}\right)\frac{1}{1-D}\frac{V_{C2}}{R} = \frac{1}{D(1-D)}\frac{V_{C2}}{R} \quad (15)$$

Equations (14) and (15) simplify the inclusion of ESRs as the inductor currents have been expressed in terms of the voltages across the capacitors that they directly connect to. By including the ESR of L_1, equation (2) becomes

$$L_1 \frac{di_{L1}}{dt} = d(v_{in} - R_{L1}i_{L1} - v_{C1}) + (1-d)(v_{in} - R_{L1}i_{L1}) \quad (16)$$

where R_{L1} is the ESR resistance of L_1. In steady state, the equation (16) becomes

$$\begin{aligned} 0 &= D(V_{in} - R_{L1}I_{L1} - V_{C1}) + (1-D)(V_{in} - R_{L1}I_{L1}) \\ &= V_{in} - R_{L1}I_{L1} - DV_{C1} \end{aligned} \quad (17)$$

By substituting (14) in (17), the ratio between the voltage across C_1 and the input voltage becomes,

$$\frac{\mathrm{V_{C1}}}{\mathrm{V_{in}}} = \frac{1}{\mathrm{D}+\frac{\mathrm{R_{L1}}}{\mathrm{D(1-D)R}}} \tag{18}$$

Similarly, the inclusion of the ESR in L_1 ($\mathrm{R_{L2}}$) leads to rewriting (3) as

$$L_2 \frac{di_{L2}}{dt} = d(v_{in} - R_{L2} i_{L2}) + (1-d)(v_{in} - R_{L2} i_{L2} - v_{C2}) \tag{19}$$

This in steady state becomes,

$$\begin{aligned} 0 &= \mathrm{D(V_{in} - R_{L2} I_{L2}) + (1-D)(V_{in} - R_{L2} I_{L2} - V_{C2})} \\ &= \mathrm{V_{in} - R_{L2} I_{L2} - DV_{C2}} \end{aligned} \tag{20}$$

Moreover, substituting (15) in (20), the ratio between the voltage across C_2 and the input voltage becomes

$$\frac{V_{C2}}{V_{in}} = \frac{1}{(1-D)+\frac{R_{L2}}{D(1-D)R}} \tag{21}$$

Finally, using equations (3.11) and (3.13), the converter's practical gain is obtained by adding (3.18) and (3.21)

$$\frac{\mathrm{V_O}}{\mathrm{V_{in}}} = \frac{1}{\mathrm{D}+\frac{\mathrm{R_{L1}}}{\mathrm{D(1-D)R}}} + \frac{1}{(1-\mathrm{D})+\frac{\mathrm{R_{L2}}}{\mathrm{D(1-D)R}}} \tag{22}$$

By construction, a smaller inductor features a smaller ESR. As explained earlier, the topology herein sizes the inductors to cancel the input current ripple at a given duty ratio. For example, if $L_2 = 3L_1$, the input current is ripple free at D = 75%. As a first approximation, it may be assumed that the inductor's ESRs follow the same trend, i.e., $\mathrm{R_{L2}} = 3\mathrm{R_{L1}}$. Figure 3.1 shows the converter's voltage gain under this assumption for different values of the ratio between the load resistance (R) and $\mathrm{R_{L2}}$. The figure is readily obtained by plotting equation (3.22). As the figure suggests, the minimum voltage gain is four and occurs at D = 50%. If the duty cycle is smaller than 50%, the gain increases again, and therefore, the minimum gain that the converter can operate is around four. The operating range is selected to be at D > 50%, which ensures that $\mathrm{L_3}$ will have enough time to discharge.

As a result, the selection of the inductors has to be such that $L_2 > L_1$, in order to achieve ripple cancelation for the input current. Furthermore, $L_2 > L_1$ implies that $\mathrm{R_{L2}} > \mathrm{R_{L1}}$., and thus, larger voltage gains are obtained for D < 10%, which can be observed in figure 3.1. This is a compromise between canceling the input current ripple and obtaining a larger voltage gain. However, in practical applications, dc/dc converters are operated at duty cycles of about 20% < D < 80%.

It can be seen from the figure that, between that range, the voltage gain is practically symmetric, and hence, the voltage gain lost is minimal. It is noteworthy that selecting D > 50% as the operating range translates into having the SC part of the converter handling a larger amount of the converter's throughput power. The figure also suggests that, as in most dc/dc converter's topologies, the inductor's ESR limits the practical gain of the approach. Therefore, this topology is more suitable if a large switching frequency is employed as, in that case, reactive components (and, hence, ESRs) are very small.

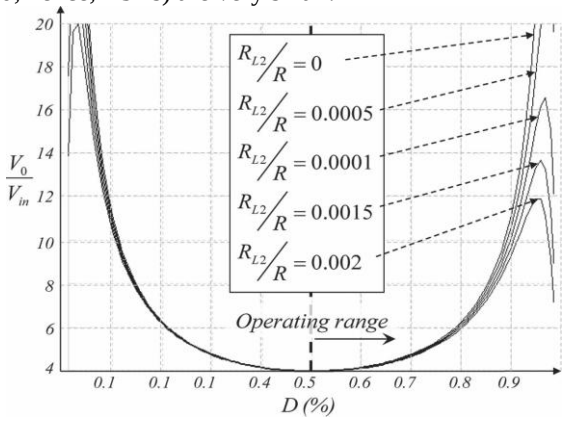


Figure 4.1: Voltage gain versus duty cycle considering inductor's ESR

4.2 Energy Storage Inductor Sizing

From figure 4, it readily follows that the current ripple on the inductor is given by

$$\Delta i_{L1} = \frac{V_{in}}{L_1}\frac{(1-D)}{F_S} \tag{23}$$

$$\Delta i_{L2} = \frac{V_{in}}{L_2}\frac{D}{F_S} \tag{24}$$

where $F_S = 1/T_S$ is the converter's switching frequency. The input current ripple, denoted by Δi_{in} , corresponds to the difference between each inductor's current ripples, i.e.,

$$\Delta i_{in} = \Delta i_{L2} - \Delta i_{L1} \tag{25}$$

$$\Delta i_{in} = \frac{V_{in}}{F_S}\left(\frac{D}{L_2} - \frac{1-D}{L_1}\right) \tag{26}$$

As it is evident from equation (26), the input current ripple can be eliminated by zeroing out the left-hand side of this equation. This leads to the following relationship:

$$L_2 = L_1\frac{D}{1-D} \tag{27}$$

For example, if the expected input and output voltages are such that the duty cycle is equal to 75%, by sizing $L_2 = 3L_1$, the input current ripple is eliminated. Once the values of L_1 and L_2 are selected, equation (26) may be used to predict the input current ripple for the full operating range. Thus, if $L_2 = 3L_1$, (26) becomes

$$\Delta i_{in} = \frac{3V_{in}}{F_S L_2}\left(\frac{4D}{3} - 1\right) \tag{28}$$

It is clear from the equation(28) that there is a linear dependence of the input current ripple with respect to the value of the duty cycle, and the assumption of ripple-free input current becomes weaker as the operating point departs from the selected duty ratio.

4.3 Peak -Current- Limiting Inductor Sizing

As mentioned earlier, the diode d_3 connects the capacitors C_2 and C_3 in parallel, and as a result, a peak- current-limiting inductor is needed. Moreover, the average current through the diode equals the load current, as it may be evident from Figure 4.1. However, the shape of the current through d_3 may be undesirable and, hence, the need to control it. In order to understand the phenomenon, consider the switching process at the time when S_2 turns off. As suggested by Figure 4.3, at that instant, capacitors C_2 and C_3 feature exactly the same voltage because they were connected in parallel. Call this voltage $V_{C.0}$. After S_2 opens, the circuit commutes into the topology in Fig. 1(b), and as a result of this, C_2 and C_3 are no longer connected. While S_2 is off (during $(1 - D)T_S$ seconds), C_3 discharges following the load current while C_2 charges following the current throughL_2. Call $V_{C3.1}$ and $V_{C3.1}$ the final voltages across capacitors C_2 and C_3, respectively. They can be expressed as

$$V_{C3.1} = V_{C.0} + \Delta v_{C2} = V_{C.0} + \frac{I_{L2}}{C_2}(1-D)T_S \tag{29}$$

$$V_{C3.1} = V_{C.0} - \Delta v_{C3} = V_{C.0} - \frac{I_0}{C_3}(1-D)T_S \tag{30}$$

At the end of $(1 - D)$ T_S, the voltage difference between them is given by

$$V_{diff} = \Delta v_{C2} + \Delta v_{C3} = \left(\frac{I_{L2}}{C_2} + \frac{I_0}{C_3}\right)(1-D)T_S \tag{31}$$

If there is no inductor in series with d_3, the peak current would be V_{diff} (some volts) over the resistance in this loop, given by the on-state resistance of S_2 and d_3, and the ESR of C_2 and C_3 (some tens of milliohms). Figure 4.2 shows a circuit schematic for the current loop where R_{eq} stands for the lumped resistance of the various elements around the loop. This may lead to a peak current that overpasses the peak current limit of the various devices in that loop.

At the time of design, this peak current can be computed using manufacturer datasheets, and thus, the inductor in series with d_3 may (or may not) be required. If the current overpasses the peak current limit of devices, the inductor is mandatory.

As shown in Figure 3.3, this current rises rapidly and may destroy power semiconductors if the inductor L_3 is not properly designed. From Figure 3.2, it is also evident that C_{eq} is the series connection of C_2 and C_3. Since L_3 stores a small amount of energy, it charges and discharges completely in a switching cycle, smoothing out the current among capacitors. However, it also produces a resonant current peak at a frequency of

$$\mathrm{f_0} = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{\mathrm{L_3 C_{eq}}}} \tag{32}$$

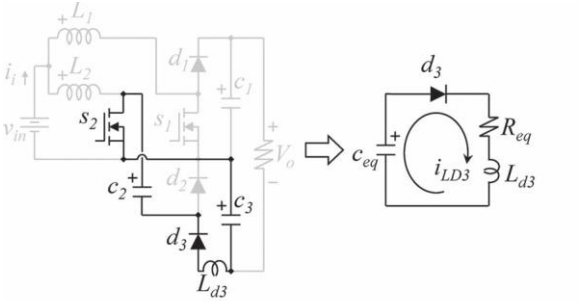


Figure 4.2: Equivalent circuit schematics

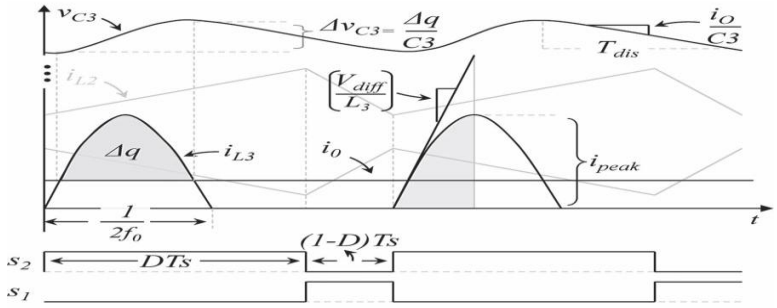


Figure 4.3: Waveforms for the reactive component selection

As mentioned above, the converter will operate at a duty cycle larger than 50%. Therefore, L_3 should be selected such that $f_0 > F_S$. This ensures that the inductor will complete the discharge process before the beginning of the next switching stage for all values of the duty cycle within the operating range. Furthermore, Figure 3.3 provides the basis for the calculation of the peak current around the loop. At the beginning of the charging period, the current starts rising at a rate of V_{diff}/L_3 . Hence, representing the current through the loop as $i_{L3}(t) = i_{L3}\sin(\omega_o t)$, its derivative at t = 0 can be computed and equated to V_{diff}/L_3. This allows solving for i_{L3}

$$\mathrm{i_{L3}} = \frac{\mathrm{V_{diff}}}{\omega_o \mathrm{L_3}} \tag{33}$$

4.4 Capacitor Sizing

The selection of the capacitance for C_1, C_2, and C_3 may be approached following a procedure analogous to that used in the sizing of the inductors L_1 and L_2. While S_1 is on, the current through C_1 follows the load current, and thus

$$\Delta \mathrm{v_{c1}} = \frac{\mathrm{I_0}}{\mathrm{C_1}}(1-\mathrm{D})\mathrm{T_S} \tag{34}$$

Also, while S_1 is closed, the capacitor C_2 charges following the current through L_2, and hence

$$\Delta \mathrm{v_{c2}} = \frac{\mathrm{I_{L2}}}{\mathrm{C_2}}(1-\mathrm{D})\mathrm{T_S} \tag{35}$$

Finally, C_3 may be selected recognizing that L_3 carries the same average current as the load. When the instantaneous value of current through this inductor overpasses the output current, the capacitor C_3 begins

charging, which leads to a voltage increase ΔV_{C3} given by $\Delta q/C_3$. This is graphically shown in Figure 3.3, where the shaded area represents the charge Δq. After L_3 has been selected, the time while C_3 is charging can be computed by finding the time at which $i_0 < i_{L3}(t)$,as suggested in Figure 3.3. Next, C_3 discharges through the remaining of the switching period, and hence

$$T_{dis} = T_S - \left(\frac{2}{\omega_0}\arcsin\left(\frac{i_0}{i_{L3}}\right)\right) \tag{36}$$

where T_{dis} corresponds to the time while C_3 discharges and arcsin represents the inverse of the sine function. Since, during this period, C_3 follows the load current, it is possible to state that

$$\Delta v_{c3} = \frac{I_0}{C_3} T_{dis} \tag{37}$$

which allows for the sizing of C_3.

V. Simulink Model and Simulation Results

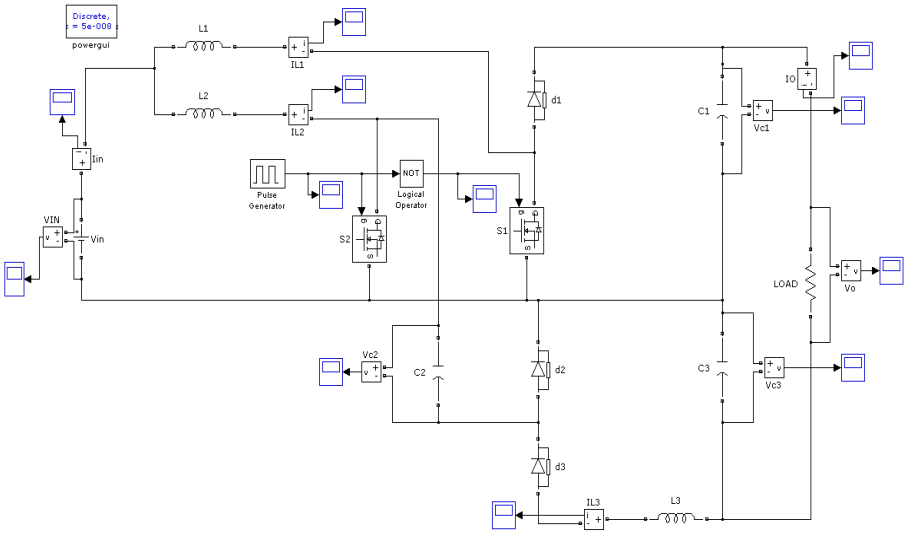
The converter presented herein was simulated in MATLAB/Simulink software in order to validate its principle of operation. The simulation circuit is as shown by the Figure 5.1. The list of parameters i.e. values of each component in the circuit is shown in the TABLE 5.1

Parameters	Values
INPUT VOLTAGE	15 V
DUTY CYCLE	70 %
OUTPUT VOLTAGE	71 V
L_2	140 µH
L_1	330 µH
L_3	28 µH
C_1, C_2, C_3	10 µF
SWITCHING FREQUENCY F_S	25 kHz

Table 5.1: Parameter specification table

5.1 Simulink Model

5.1.1 Novel Boost Converter Topology



5.2 Simulation Results- Waveforms

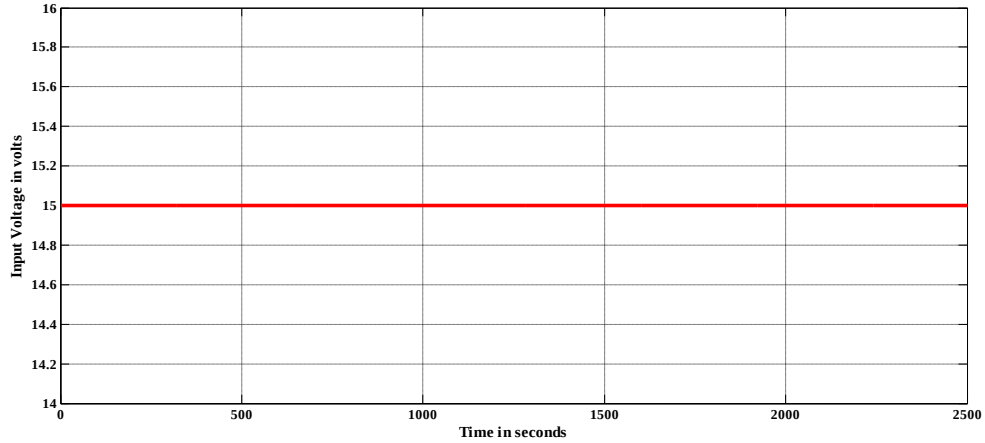


Figure 5.1: Waveform of input voltage

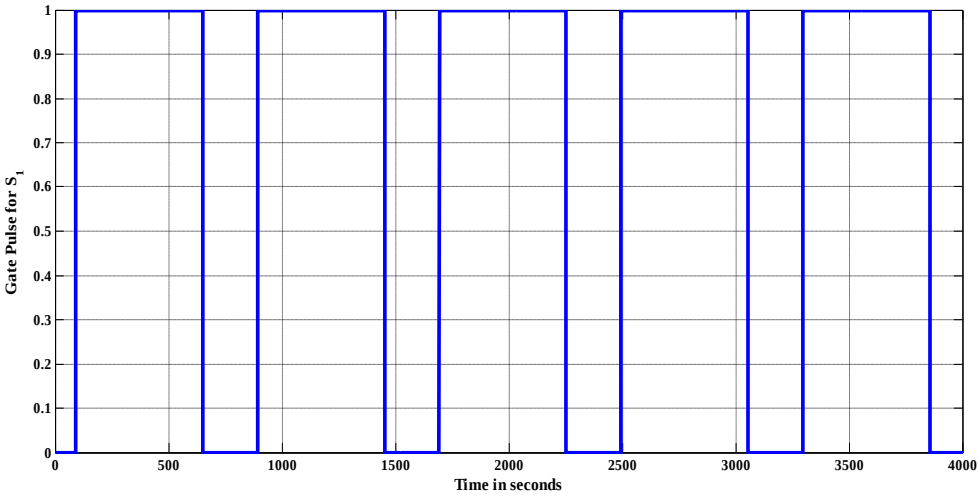


Figure 5.2: Gate pulse for switch S_1

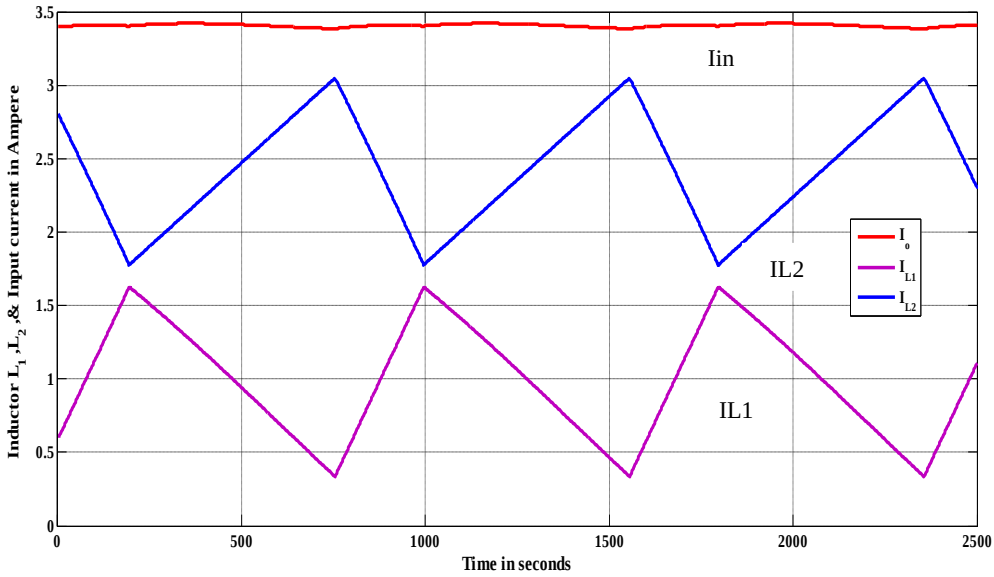


Figure 5.3: Waveforms of current through inductors and input current

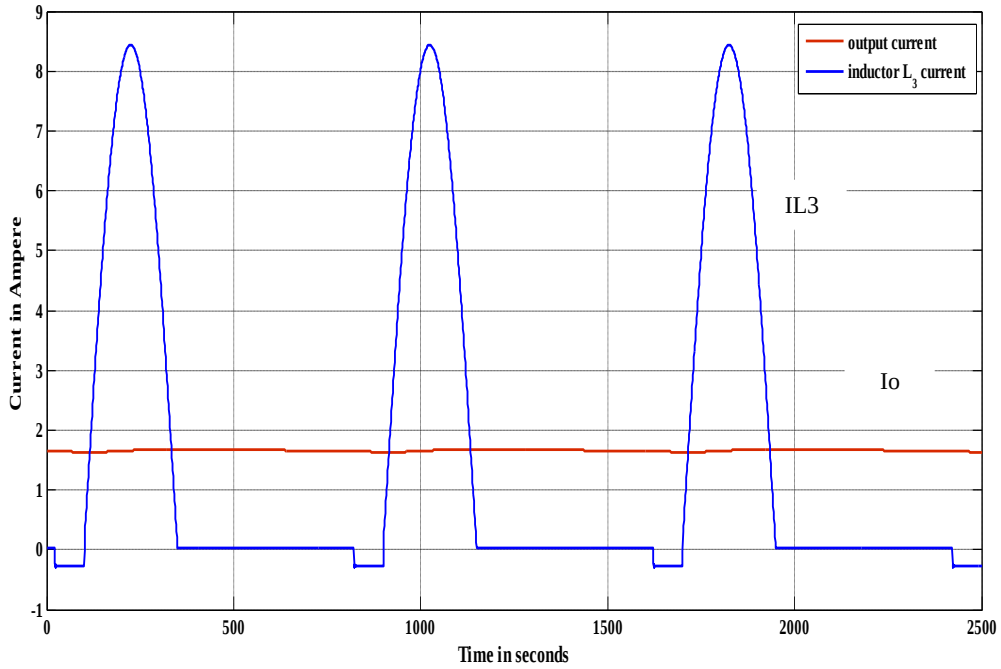


Figure 5.4: Waveforms of current through resonant inductor and output current

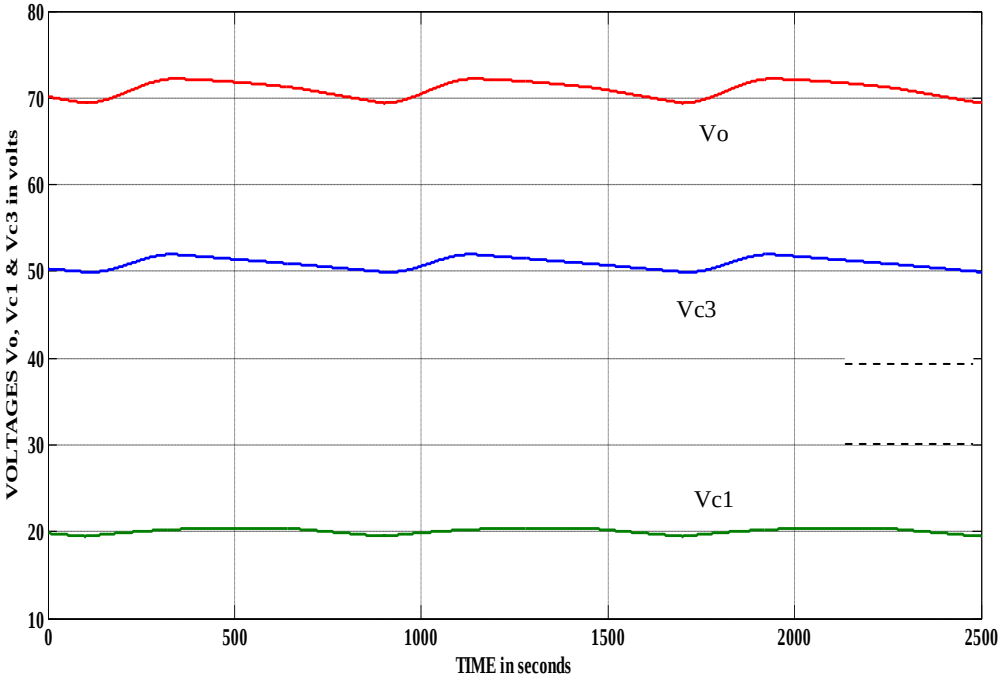


Figure 5.5: Waveforms of voltages through capacitors and output voltage

It is evident from the simulation results that the input current is almost ripple free. A closer examination of the measurements also suggests the simulation datas are consistent with the values obtained as per the design.

VI. Conclusion

This paper has presented a boost dc–dc converter topology, with the novel capability of canceling the input current ripple at an arbitrarily preselected duty cycle. This is accomplished without increasing the count of the number of components. In addition, the converter features a high voltage gain without utilizing extreme values of duty cycle or boosting transformers. These features make the converter ideal to process electric power coming from low-voltage power-generating sources, such as renewable. The boost factor or voltage gain may be extended by utilizing diode-capacitor multipliers. Those features are highly desirable in fuel cell applications.

Moreover, the rapid development of silicon carbide and other wide-band gap fast-switching power semiconductors will enable the use of smaller reactive components and hence provide further advantages to the approach presented herein against transformer or coupled-inductor-based topologies. Simulation results are consistent with the analytical predictions of the various formulas developed through this paper, and hence, the approach may be considered definitely validated.

6.1 Scope for Future Work

The presented converter can be extended to a multiplier boost converter. An advantage of this topology is that helps to reduce the size of the input inductor and its corresponding series resistance. The converter presented is designed in such a way that both switches are operated alternatively. However, they can also be operated with the same duty cycle in an interleaving manner. In this particular case, both output capacitors would obtain the same voltage and thus output voltage can be doubled.

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