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A New 5 Level Inverter for Grid Connected Application

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Abstract: *A five-level inverter is developed and applied for injecting the real power in to the grid to reduce the switching power loss, harmonic distortion, and electromagnetic interference caused by the switching operation of power electronic devices. Two dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter configure the five-level inverter. The input of the dual-buck converter is two dc capacitor voltage sources. The dual-buck converter converts two dc capacitor voltage sources to a dc output voltage with three levels and balances these two dc capacitor voltages. The output voltage of the dual-buck converter supplies to the full-bridge inverter. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility voltage to convert the output voltage of the dual-buck converter to a five-level ac voltage. The output current of the five-level inverter is controlled to generate a sinusoidal current in phase with the utility voltage to inject into the grid.*

Keywords: *Carrier, Filter, Five-level, THD, Voltage balance.*

I. Introduction

Energy scenario is changing. The intensified research on renewable energy has lead to the emergence of a new era where renewable energy resources like solar, wind etc play the lead role. The use of hazardous fossil fuels has become obsolete. The birth of semiconductor technology and its widespread acceptance and applications fuelled the design of various power converter topologies. It has become the key responsibility of these converters to integrate the renewable energy sources in to the grid with required efficiency.

However, there exist a tough competition between classic power converter topology using high voltage semiconductor and new converter topologies like multilevel inverters using medium voltage semiconductors. Nowadays multilevel converters prove to be a good solution to power application due to the fact that they can achieve high power using medium power semiconductor devices.

Multilevel converters present great advantage when compared with two level converters. These advantages are fundamentally focused on improvement in output signal quality. As the number of level increase, the THD in the inverter output remain less when compared to two level inverters. The electromagnetic interference is also minimized.

While bestowing all these advantages, the multilevel converters bear some limitations too. The control of the converter is complex when compared to conventional topologies. Balancing of dc capacitor voltage, high switching losses still remain a serious issue.

The most common multilevel converter topologies are the neutral point clamped (NPC), flying capacitor (FC), cascaded H-bridge(CHB). These converters present widespread applications in ac motor drives such as in conveyors, pumps, fans etc. Cascaded H-bridge has been successfully commercialized for very high power and power quality demanding applications up to range of 31MVA due to its series expansion capabilities.

This paper reveals the working and simulation of a new 5 level inverter topology which proves to overcome some of the limitations of conventional multilevel topologies.

II. Proposed Topology

This five-level inverter is configured by two dc capacitors, a dual buck converter, a full-bridge inverter, and a filter. The dual-buck converter is configured by two buck converters. The two dc capacitors perform as energy buffers between the dc–dc converter and the five-level inverter. The output of the dual-buck

converter is connected to the full-bridge inverter to convert the dc voltage to ac voltage. An inductor is placed at the output of the full bridge inverter to form as a filter inductor for filtering out the high-frequency switching harmonic generated by the dual-buck converter.
The block schematic is shown in Fig 2.1 and circuit is shown in Fig 2.2

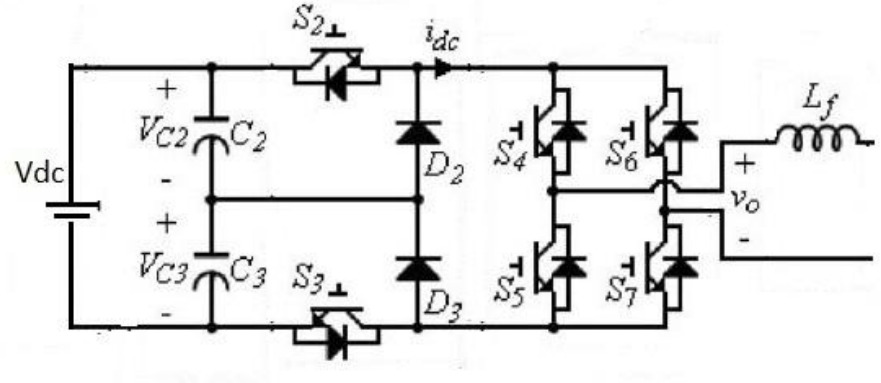

Figure 2.2.Circuit of proposed topology

2.1 Operating Principle

The operation of this five-level inverter can be divided into eight modes. Modes 1–4 are for the positive half-cycle, and modes 5–8 are for the negative half-cycle. The power electronic switches of the full-bridge inverter are switched in low frequency and synchronously with the utility voltage to convert the dc power into ac power for commutating. The power electronic switches S4 and S7 are in the ON state, and the power electronic switches *S*5 and *S*6 are in the OFF state during the positive half-cycle. On the contrary, the power electronic switches S4 and S7 are in the OFF state, and the power electronic switches *S*5 and *S*6 are in the ON state during the negative half-cycle. Since the dc capacitor voltages VC2 and VC3 are balanced by controlling the five-level inverter, the dc capacitor voltages VC2 and VC3 can be represented as shown in equation (1):

VC2 = VC3 =1/2Vdc (1)

The operation modes of this five-level inverter are stated as follows.
Mode 1: Fig 2.3 shows the operation circuit of mode 1.
The power electronic switch of the dual-buck converter S2 is turned ON and S3 is turned OFF. DC capacitor C2 is discharged through S2, S4 , the filter inductor, the utility, S7 , and D3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are Vdc/2.

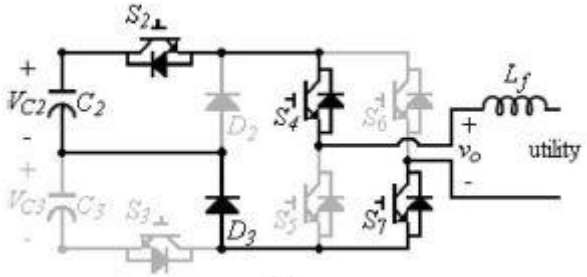

Figure 2.3 Mode 1 operation

Mode 2: Fig 2.4 shows the operation circuit of mode 2.
The power electronic switch of the dual-buck converter *S*2 is turned OFF and *S*3 is turned ON. DC capacitor *C*3 is discharged through D2, *S*4 , the filter inductor, the utility, *S*7 , and *S*3 to form a loop. Both output voltages of the dual-buck converter and five level inverter are Vdc/2.

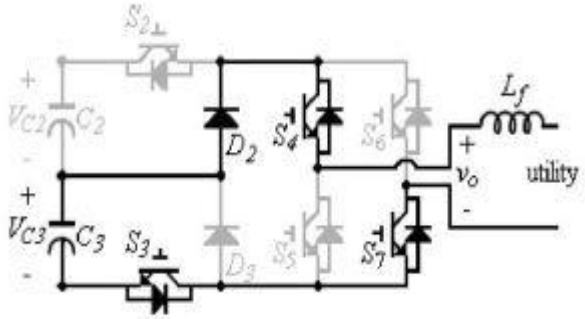

Figure 2.4 Mode 2 operation

Mode 3: Fig 2.5 shows the operation circuit of mode 3.
Both power electronic switches *S*2 and *S*3 of the dual-buck converter are turned OFF. The current of the filter inductor flows through the utility, S7, D3, D2, and *S*4. Both output voltages of the dual buck converter and five-level inverter are 0.

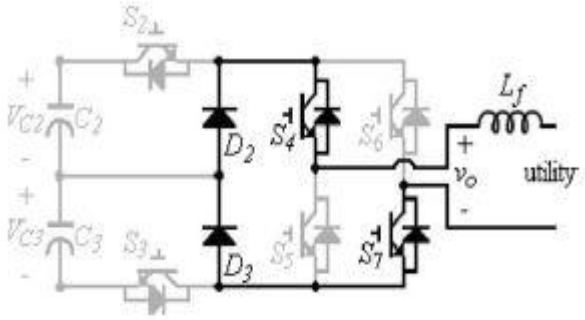

Figure 2.5 Mode 3 operation

Mode 4: Fig 2.6 shows the operation circuit of mode 4. Both power electronic switches S2 and S3 of the dual-buck converter are turned ON. DC capacitors C2 and C3 are discharged together through *S*2, *S*4, the filter inductor, the utility, S7, and S3 to form a loop. Both output voltages of the dual-buck converter and five-level inverter are Vdc.

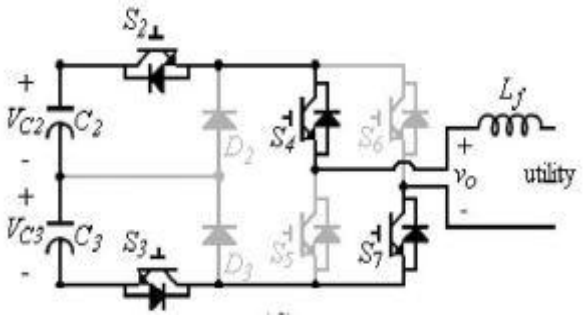

Figure 2.6 Mode 4 operation

Modes 5–8 are the operation modes for the negative half cycle shown in Fig 2.7 to Fig 2.10. The operations of the dual-buck converter under modes 5–8 are similar to that under modes 1–4, and the dual-buck converter can also generate three voltage levels Vdc/2, Vdc/2, 0,and Vdc, respectively. However, the operation of the full-bridge inverter is the opposite. The power electronic switches *S*4 and *S*7 are in the OFF state, and the power electronic switches *S*5 and *S*6 are in the ON state during the negative half-cycle. Therefore, the output voltage of the five-level inverter for modes 5–8 will be −Vdc/2, −Vdc/2, 0, and −Vdc, respectively. Considering operation modes 1–8, the full-bridge inverter converts the dc output voltage of the dual-buck converter with three levels to an ac output voltage with five levels which are Vdc, Vdc/2, 0, −Vdc/2, and −Vdc.

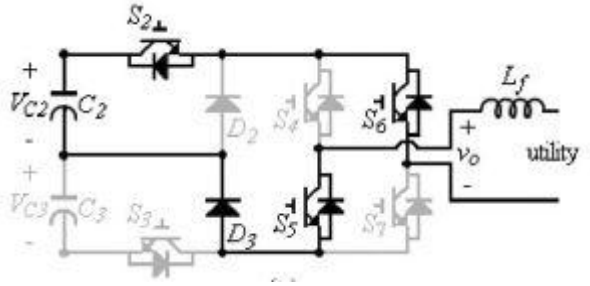

Figure 2.7 Mode 5 operation

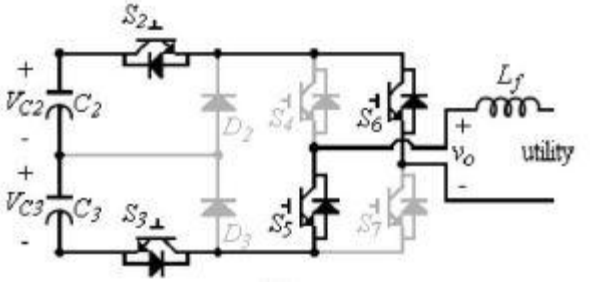

Figure 2.8 Mode 6 operation

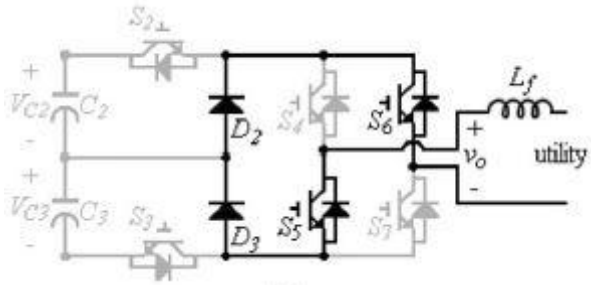

Figure 2.9 Mode 7 operation

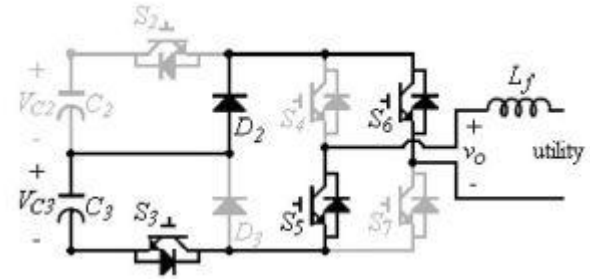

Figure 2.10 Mode 8 operation

The operation of power electronic switches *S*2 and *S*3 should guarantee the output voltage of the dual-buck converter is higher than the absolute of the utility voltage. The waveforms of output voltage of five-level inverter and utility voltage are shown in Fig 2.11.

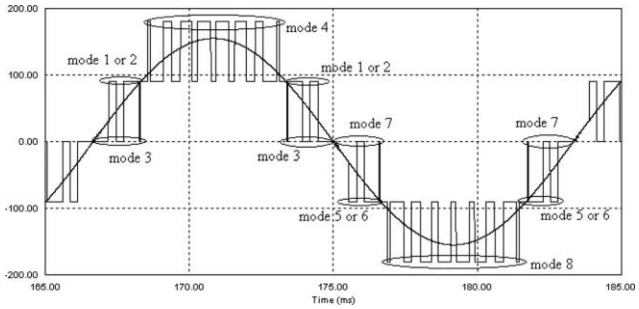

Figure 2.11 Overall operation of 5 level inverter

Due to the operation of full-bridge inverter, the voltage and current in the dc side of full-bridge inverter are their absolute values of the utility voltage and the output current of the five level inverter. When the absolute of the utility voltage is smaller than Vdc/2, the output voltage of the dual-buck converter should change between Vdc/2 and 0. Accordingly, the power electronics of five-level inverter is switched between modes 1 or 2, and mode 3 during the positive half-cycle. On the contrary, the power electronics of five-level inverter is switched between modes 5 or 6, and mode 7 during the negative half-cycle. One of the power electronic switches S2 and S3 is in the OFF state and the other is switched in high frequency during one PWM period.

2.2 Voltage Balance of Five-Level Inverter

Balancing the voltages of dc capacitors is very important in controlling the multilevel inverter. The voltage balance of dc capacitor voltages VC2 and VC3 can be controlled by the power electronic switches S2 and S3 easily. When the absolute of the utility voltage is smaller than Vdc/2, one power electronic switch either *S*2 or *S*3 is switched in high frequency and the other is still in the OFF state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages VC2 and VC3. If dc capacitor voltage VC2 is higher than dc capacitor voltage VC3, power electronic switch *S*2 is switched in high frequency. In this situation C2 will be discharged.

Thus, the dc capacitor voltages VC2 decreases. On the contrary, power electronic switch *S*3 is switched in high frequency when voltage VC3 is higher than voltage VC2. Thus, the dc capacitor voltages VC3 decreases. In this way, the voltage balance of C2 and C3 can be achieved. When the absolute of the utility voltage is higher than Vdc/2, one power electronic switch either S2 or S3 is switched in high frequency and the other is still in the ON state.

Which power electronic switch is switched in high frequency depends on the dc capacitor voltages VC2 and VC3. If dc capacitor voltage VC2 is higher than dc capacitor voltage VC3, the power electronic switch S3 is switched in high frequency.

When the power electronic switch S3 is turned ON, both C2 and C3 are discharged. However, only C2 supplies the power when the power electronic switch S3 is turned OFF. Thus, C2 will discharge more power than that of C3. On the contrary, the power electronic switch *S*2 is switched in high frequency when dc capacitor voltage VC3 is higher than dc capacitor voltage VC2. When the power electronic switch S2 is turned ON, both C2 and C3 are discharged. However, only C3 supplies the power when the power electronic switch S2 is turned OFF. Thus, C3 will discharge more power than that of C2. In this way, the voltage balance of C2 and C3 can be achieved. The voltages of capacitors C2 and C3 can be easily balanced compared with the conventional multilevel inverter.

2.3 Comparison with Conventional 5 Level Topologies

Table 1: Comparison with Conventional 5 Level Topologies

	Diode clamped	Flying capacitor	Cascaded H-bridge	Developed topology
Power electronics	8	8	8	6
Capacitors	2	4	2	2
Voltage balance of capacitors	hard	hard	hard	easy
High frequency switches	8	8	8	2

III. Inverter Control

The five-level inverter performs the functions of converting the dc power into high-quality ac power and injecting it into the utility, balancing two dc capacitor voltages VC2 and VC3.

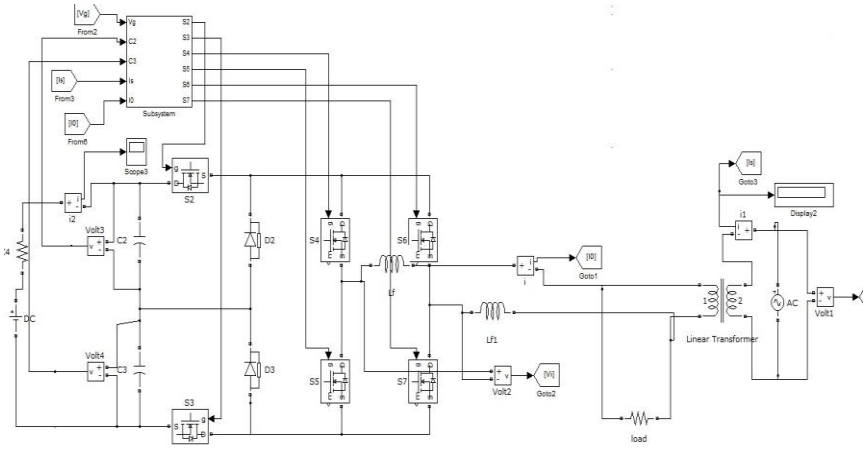

Figure 3.1 Main circuit configuration

Fig 3.2 shows the control block diagram of five-level inverter. In the operation of the five-level inverter, the dc bus voltage must be regulated to be larger than the peak voltage of the utility, and the dc capacitor voltages of C2 and C3 must be controlled to be equal. Besides, the five-level inverter must generate a sinusoidal current in phase with the utility voltage to be injected into the utility.

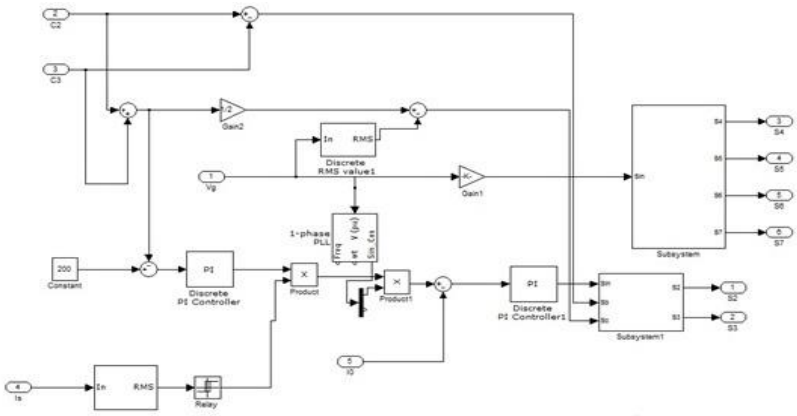

Figure 3.2 Control of 5 level inverter

A multilevel carrier based PWM technique is utilized to generate the switching signal for switches S2 and S3. For an m-level inverter, (m-1) carriers with the same frequency fc and same peak-to-peak amplitude Ac are disposed such that the bands they occupy are contiguous. The reference, or modulation waveform has peak-to-peak amplitude Am and frequency fm, and it is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals the switching pulses are generated according to the switching logic. The carrier has a frequency of 20kHz.

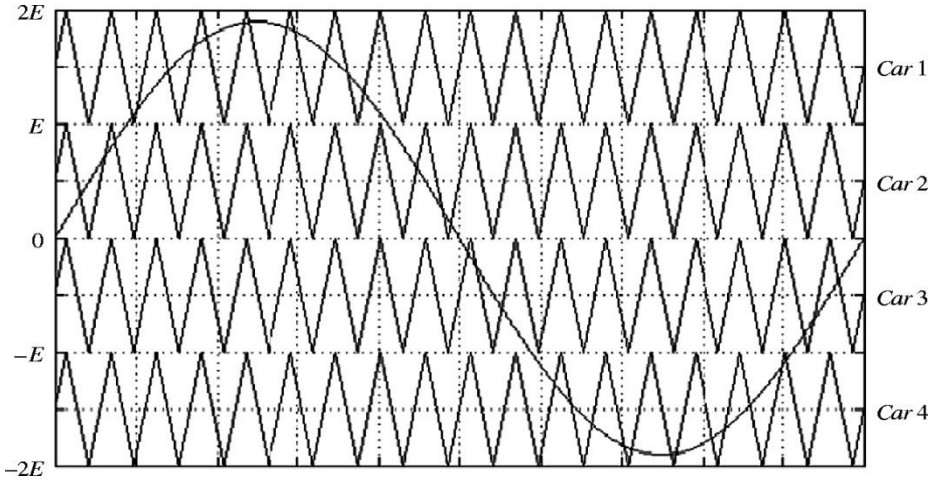

Figure 3.3 Carrier and reference signal comparison

The detected utility voltage is also sent to a comparator to obtain the switching signal for the full bridge inverter switches S4 to S7. These switches are switched in utility frequency. For positive half cycle switches S4 and S7 are turned ON. For negative half cycle switches S5 and S6 are turned ON. As mentioned earlier, only two power electronic switches S2 or S3 in the five-level inverter should be switched in high frequency, and only one of them is switched in high frequency at any time, and the voltage level of every switching is Vdc/2. Therefore, the five-level inverter can reduce the switching loss effectively. Overall switching states of inverter is shown in Table 2.

Table 2.Overall switching states of inverter

S2	S3	S4	S5	S6	S7	Vout
1	1	1	0	0	1	+Vdc
1	0	1	0	0	1	+Vdc/2
0	1	1	0	0	1	+Vdc/2
0	0	1	0	0	1	0
0	0	0	1	1	0	0
1	0	0	1	1	0	-Vdc/2
0	1	0	1	1	0	-Vdc/2
1	1	0	1	1	0	-Vdc

IV. Simulation Results

The proposed model was simulated in MATLAB/Simulink. The grid voltage was chosen to be 110V and the DC voltage was chosen as 165V since it must be greater than peak of grid voltage. Waveforms of grid voltage, inverter output current, inverter output voltage and capacitor voltages were obtained. Fig 4.1 shows the grid voltage waveform. Fig 4.2 shows inverter output current which is obtained with 20 % current ripple by using a filter inductor of 5mH. The THD of inverter current was found to be 3.0%. Fig.4.3 shows waveform of inverter output voltage. THD was found to be 8.83%. Fig.4.4 shows the combined waveform of grid voltage and inverter output voltage. Fig 4.5 shows the combined waveform of inverter current and grid voltage. The voltage of dc link capacitors shown in Fig 4.6 were found to be balanced and each of the two capacitors stores 82.5V with a voltage ripple of 0.13%. The power factor was found to be 0.9903.

Table 3 :Parameters used in simulation

DC bus capacitor (C_2 and C_3)	2,200 µ F
Filter inductor (L_f)	5mH
DC bus setting voltage	170V
Switching frequency(PWM)	20kHz
Utility voltage	110V
Utility frequency	60Hz
Load resistor	100Ω

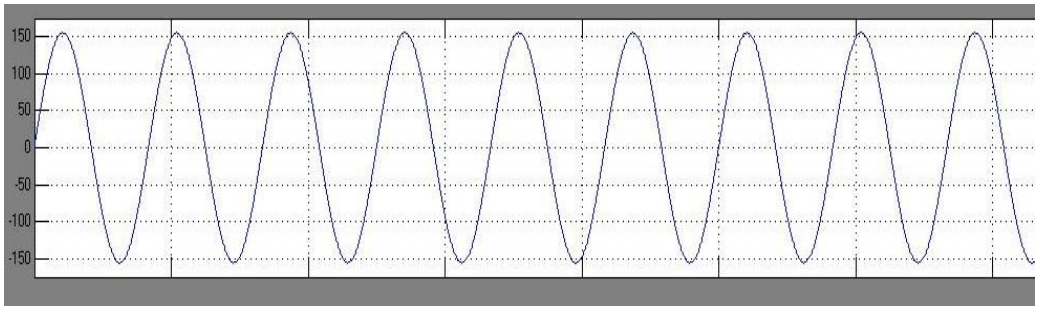

Figure 4.1. Grid voltage waveform

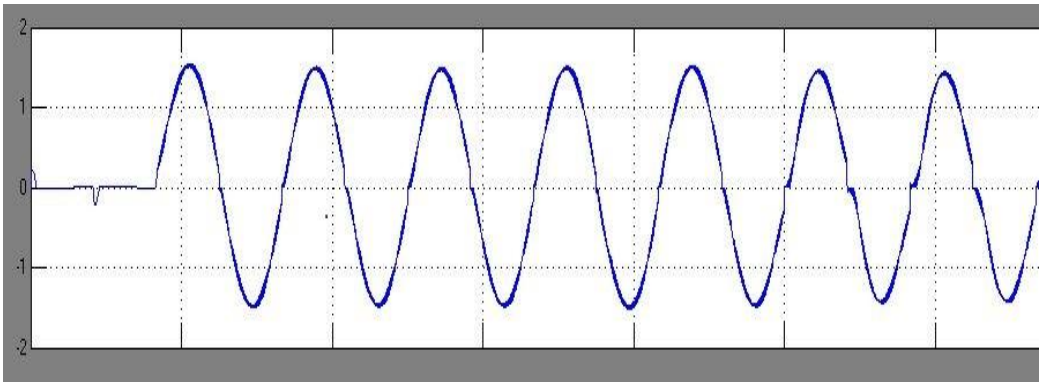

Figure 4.2. Inverter output current waveform

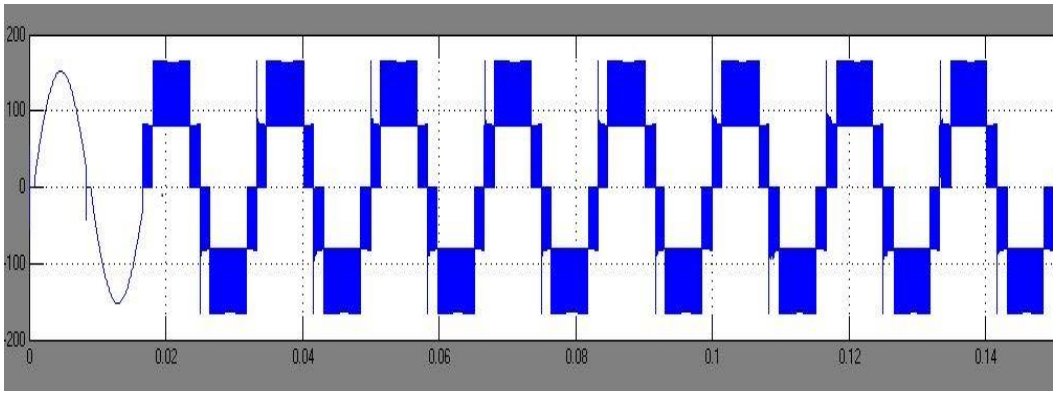

Figure 4.3. Inverter output voltage waveform

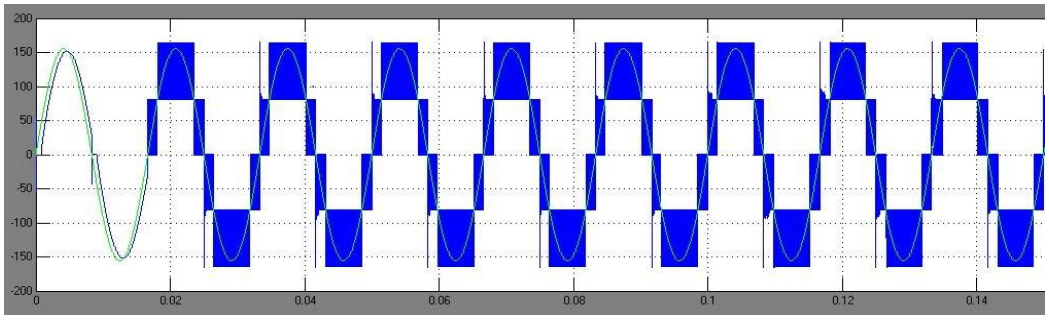

Figure 4.4. Inverter output voltage and grid voltage waveform

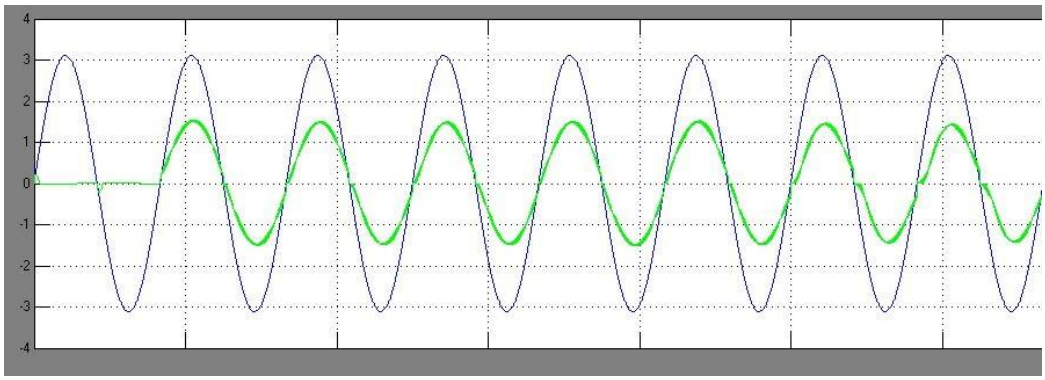

Figure 4.5. Inverter output current and grid voltage waveform

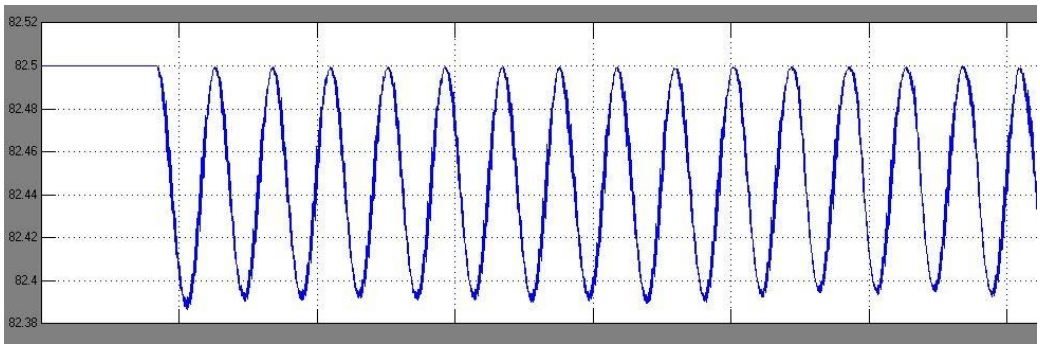

Figure 4.6. DC link capacitor voltage waveform

V. Conclusion

Proposed 5 level inverter was simulated and necessary waveforms were obtained. Waveforms of grid voltage, inverter current, voltage, capacitor voltage etc were obtained. The capacitor voltage was found to be almost balanced. The THD of inverter current and voltage were verified. THD was found to be less than 5%. The power factor of the system was found to be above 0.9. The switching losses will be less when compared to conventional topologies since less number of power electronic switches are used .Thus as a whole the proposed 5 level inverter is found to have good performance under grid connected application.

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