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# Implementation of Wide Band Frequency Synthesizer Base on DFS (Digital Frequency Synthesizer) Controller Using VHDL

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***Abstract:*** *A frequency synthesizer is an electronic system for generating any of a range of frequencies from a single fixed time base or oscillator. They are found in many modern devices, including radio receivers, mobile telephones, radiotelephones, walkie-talkies, CB radios, satellite receivers, GPS systems, etc. Direct Digital Synthesis (DDS) is a kind of frequency synthesizer that use electronic methods for digitally creating arbitrary waveforms and frequencies from a single, fixed source frequency. Direct Digital Frequency Synthesis (DDFS) is a mixed signal part i.e. it has both digital and analog parts. DDFS's digital part is also known as Numerically Controlled Oscillator (NCO), which consists of a Phase Register, a Phase Accumulator (PA) and a ROM. The analog part has Digital-to-Analog Converter and a filter. NCO is a digital computing block which renders digital word sequences in time at a given reference clock frequency, which thereafter are converted into analog signals to serve as a synthesizer. The phase accumulator (PA) clocked with, generates the phase value sequence. Application of the DDFS ranges from instrumentation to modern communication systems, which employs spread-spectrum and phase shift-keying modulation techniques.*

*The focus of this paper is on design, analysis and simulation of DDFS, using tools like Xilinx and Cadence. Traditional designs of high bandwidth frequency synthesizers employ the use of a phase locked- loop (PLL). DDFS provides many significant advantages over the PLL approaches, such as fast settling time, sub-Hertz frequency resolution, continuous-phase switching response and low phase noise.*

***Keywords:*** *DFS, Modelsim 10.2a, VHDL, Wide Band Frequency Synthesizer, Xilinx ISE 14.2.*

## I. INTRODUCTION

Wide Band Frequency Synthesizer has become essential components in wireless communication systems. They are used as frequency synthesizers with precise and convenient digital control in both traditional electronics, such as televisions and AM/FM radios, and modern consumer products among which cellular mobile phone is a striking example.

IC fabrication technology advances have made monolithic integration possible. More and more electronic devices can be put on the same chip to reduce the number of external components and then the costs. Therefore, on a single chip we can accomplish many functions for which we might need to make several chips work together a few years ago. A monolithic wide-band PLL is of great interests to wireless communication applications due to both its low cost and convenience to switch between different communication standards. The focus of this work is to implement a wide-band Frequency Synthesizer using as few as possible building blocks and also as simple as possible structure.

Many of the concepts of DDS are illustrated by the way in which a sine wave is generated. The figure below shows a block diagram of a simple DDS function generator. The sine function is stored in a RAM table. The RAM's digital sine output is converted to an analog sine wave by a DAC. The steps seen at the DAC output are filtered by a low pass filter to provide a clean sine wave output.

The frequency of the sine wave depends on the rate at which addresses to the RAM table are changed. Addresses are generated by adding a constant, stored in the phase increment register (PIR), to the phase accumulator. Usually, the rate of additions is constant, and the frequency is changed by changing the number in the PIR.

Our intuition might suggest that a large number of samples are required for each cycle of the sine wave to achieve good spectral purity of the output. A sketch of a sine which is approximated by a small number of samples per cycle hardly looks like a sine wave. Remarkably, only about three samples are required during each cycle. In fact, if we could make an arbitrarily sharp, low-pass filter, we would need only two samples per cycle

## II. RELATED WORK

The Fast frequency switching is crucially important in modern wireless communication systems such as TDMA/CDMA digital cellular systems and spectrum-spread wireless LANs. For example, the TDMA system may require that the carrier frequency have to be switched during a signal slot, that is, the change must be accomplished within 100us. Linear phase shifting is also crucial in any system that uses phase shift keying modulation techniques. Such system includes IS-95, IS-94, GSM, DCS-1800, CDPD and several others. Direct Digital Frequency Synthesizer (DDFS) can achieve fast frequency switching in small frequency steps, over a wide band. Also it provides linear phase and frequency shifting with good spectral purity. So, DDFS is best suited to use in the above communication systems. A further requirement for DDFS is low power consumption budget, especially for portable wireless terminals.

Woogeun Rhee et al (2013), worked on overview of fractional- N phase-locked loops (PLLs) with practical design perspectives focusing on a 0Σ modulation technique and a finite-impulse response (FIR) filtering method. Spur generation and nonlinearity issues in the 0Σ fractional-N PLLs are discussed with simulation and hardware results. High-order 0Σ modulation with FIR-embedded filtering is considered for low noise frequency generation. Also, various architectures of finite-modulo fractional-N PLLs are reviewed for alternative low cost design, and the FIR filtering technique is shown to be useful for spur reduction in the finite-modulo fractional-N PLL design [2].

Govind S. Patel et al (2013), worked on an optimized Direct Digital Frequency Synthesizer (DDFS) utilizing Piecewise Linear Approximation is introduced. The proposed technique allows successive read access to memory cells per one clock cycle using time sharing. The output values will be temporarily stored and read at a later time. The output of this system is a reconstructed signal that is a good approximation of the desired waveform. As a result, the DDFS only needs to store fewer coefficients and the hardware complexity is significantly reduced. The proposed DDFS has been analyzed using MATLAB. The SFDR of synthesized achieved is 84.2 dBc. To prove the better performance of proposed DDS architecture it is compared favorably with several existing DDS architectures. In future it can also be used to improve the performance of Hybrid DDS-PLL Synthesizers [3].

M. NourEldin M. et al (2013), proposed a algorithm for a low-power high-resolution ROM-less Direct Digital frequency synthesizer architecture based on FPGA Design is proposed. This work is equipped to generate a sinusoidal waveform with a new simple design method, which is endowed with high speed, low power and high spurious free dynamic range (SFDR) features. The proposed low power methodology is achieved by two methods: first, in a phase accumulator design by selecting a pipelined phase accumulator with 8-bit components that has lowest number of four input LUTs and number of occupied Slices. Second, in the circuit of TSC by proposing the circuit without an external power source. The output frequency of proposed design is 195.35 kHz using built in clock frequency of 50MHz. However, the maximum operating frequency is 190.93MHz. In addition, the design has frequency resolution of 0.012Hz, which is promising to get very high tuning frequency with SFDR of 42 dBc or 70 dBFS [4].

Eli Bloch wt al, (2013), worked on an integrated circuit (IC) for heterodyne optical phase locking in a 1–20-GHz offset range is hereby reported. The IC, implemented in a 500-nm InP HBT process, contains an emitter coupled logic digital single-sideband mixer to provide phase locking at a 20-GHz offset frequency, and a wideband phase-frequency detector designed to provide loop acquisition up to 40-GHz initial frequency offset. The all-digital IC design has phase-frequency detection gain independent of IC process parameters or optical signal levels, and provides a wide offset locking range. A 100-ps delay decreases the overall loop delay, making wideband loop filter design possible. In addition, a medium-scale high-frequency logic design methodology is presented and fully discussed [5].

Jochen Rust et al, (2012) said that nowadays Direct Digital Frequency Synthesizers (DDFS) are used in a vast area of applications, the demand for simple and efficient hardware design and implementation methods is a highly important aspect. In this work a new approach is introduced considering Automatic Nonuniform Piecewise linear function Approximation (ANPA). Automatic function generation is performed that enables quick HDL design by parameter specification in advance. For evaluation, several different configurations are simulated regarding approximation accuracy and complexity. In addition, logical and physical IC synthesis is performed for selected designs and their results are compared with actual references with respect to the common hardware constraints power, area and time [6].

## III. METHODOLOGY

The concept of this technique is the same with that used in above quadrant compression technique [3]. Figure 1 shows the block diagram of the proposed DDFS architecture. The MSB2 is used to select the quadrants of the sine wave, while the MSB1 is used to control the format converter. The remaining W-2 bits are fed into Complement or whose output is split into two parts, the MSB part, with A bits long, represents the S segments and the LSB part with B bits long, represents an angle x in the interval [0,π/ (2S)]. A multiplexer and its coefficients are the equivalent of a ROM which provide the segment initial amplitudes Qi, represented with D bits. The proposed architecture also incorporates pulse forming circuit which controls the fetching and loading process of successive Qi coefficients. This circuit along with the three storage registers and one Subtract or is essential to perform the task of the slope derivation during the segment interval. Besides the sine symmetry property, the linear approximation method has been used to approximate the first quadrant of sine function by S straight lines; each line is defined by two coefficients, Pi and Qi. The coefficient Mi, which represents the slope of ith element. The first quadrant of sine function approximation segment can be calculated from the sine function as follows.

$$\boldsymbol{Pi = \{\sin [i\Delta x] - \sin [(i-1)\,\Delta x]\}/\,\Delta x \;\; 1 \le i \le S} \qquad \textbf{(1)}$$

where, Δx = the length of segment. Above Eq. (1) can be realized easily by subtracting the Sin [i.Δx] at successive phase angles and then dividing the result by Δx.

As Δx unsigned constant coefficient, the division can simply be realized by binary operation. The coefficients Qi, is equal to [sin (i-1) Δx] points, As examples for segment number1, (Q1= 0), yields K1 = P1x and for segment number 2, (Q2 = sin Δx), in general, Qi = sin [(i-1) Δx] for the ith segment and it can be realized by delaying the pervious sin (iΔx) by one clock period, hence the realization of the whole Ki (x) function is accomplished. It is clear that it must get two consecutive sine points at the same time to conduct the process of subtraction and extraction of the slope later.

These two sine points can be got only when the corresponding phase angles point simultaneously to their addresses in the sine LUT and that is an inconsequent assumption. As mentioned earlier, the accessing of the memory is valid only once at a specific clock cycle. In this study, we introduce architecture of pulse forming circuit which is performing the task of time sharing and propose the procedure enumerated below to get around this problem. The value of phase register at any clock period represents the phase of the sine function. As not all of the samples of the sinusoid are stored, only the first A bits of the W-2 phase accumulator output are used to select segment initial amplitudes Qi. , i.e., it represents the MUX address inputs. The remaining B LSB's bits (B = W-2-A) represent an angle x in the interval Δx and are used to calculate the value of the interpolated sine point. It has three simple blocks: digital comparator, pulse narrowing circuit and tapped delay.

- At each clock cycle, the digital comparator examines the MUX Address inputs for detecting the changes in data select inputs i.e., transitions between the segments
- The detected signal will be applied to the Pulse Narrowing Circuit to produce a Δt pulse width signal i.e., trigger1 (tg1), which is usually a fraction of 1/fclk
- This signal, tg1 gives an order to advance the Data Select Inputs of MUX by 1, hence the output of the MUX during this time slot is Sin [(i+2)Δx]
- At the same time, the tg1 is used to load this value in register1 (R1)
- After Δt, the data select inputs get back to the previous address value, so the output of MUX will be Sin [(i+1)Δx]
- Trigger2 (tg2) enables register 2 (R2) to load this value
- The content of R2 will be subtracted from the content of R1 and the result will be loaded in register3 (R3), after a specific time which is precisely sufficient to give a chance for signals to be propagated through all gates and settle. Hence, the slope is simply derived and kept unchanged during the segment interval.

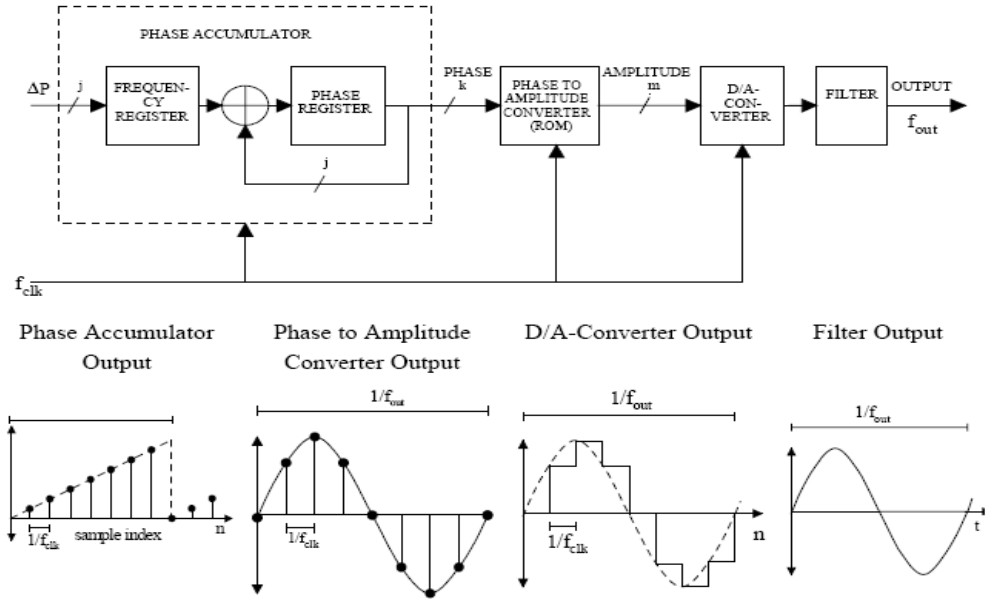


Fig 1: Block diagram of a direct digital frequency synthesizer

As shown in Figure 1, the main components of a DDFS are a phase accumulator, phase-to-amplitude converter (a sine look-up table), a Digital-to-Analog Converter and filter. A DDFS produces a sine wave at a given frequency. The frequency depends on three variables; the reference-clock frequency and the binary number programmed into the phase register (frequency control word,clkfM), length of n-bit accumulator. The binary number in the phase register provides the main input to the phase accumulator.

If a sine look-up table is used, the phase accumulator computes a phase (angle) address for the look-up table, which outputs the digital value of amplitude—corresponding to the sine of that phase angle—to the DAC. The DAC, in turn, converts that number to a corresponding value of analog voltage or current. To generate a fixed-frequency sine wave, a constant value (the phase increment—that is determined by the binary numberM) is added to the phase accumulator with each clock cycle. If the phase increment is large, the phase accumulator will step quickly through the sine look-up table and thus generate a high frequency sine wave. If the phase increment is small, the phase accumulator will take many more steps, accordingly generating a slower waveform.

**Building Blocks of DDFS:**

A DDFS is a mixed signal device i.e. it has both analog and digital blocks. These blocks are the Phase Register, Phase Accumulator, Phase-to-Amplitude Converter (ROM/LUT), Digital-to-Analog Converter, and Reconstruction Filter. The functionality of each of these blocks is discussed in the following section.

**Phase Accumulator**:

Continuous-time sinusoidal signals have a repetitive angular phase range of 0 to 360 degrees. The digital implementation is no different. The counter's carry function allows the phase accumulator to act as a phase wheel in the DDFS implementation.

**Phase-to-Amplitude Converter (ROM/ LUT):**

The DDFS's ROM is a sine Look up Table; it converts digital phase input from the accumulator to output amplitude. The accumulator output represents the phase of the wave as well as an address to a word, which is the corresponding amplitude of the phase in the LUT. This phase amplitude from the ROM LUT drives the DAC to provide an analog output. It is also called a digital Phase-to-Amplitude Converter (PAC)

**Digital-to-Analog Converter and Filter:**

The phase accumulator computes a phase (angle) address for the look-up table, which outputs the digital value of amplitude—corresponding to the sine of that phase angle—to the DAC. The DAC, in turn, converts that number to a corresponding value of analog voltage or current.

## IV. SIMULATION RESULTS

We are generating the sine wave of 1 Hz frequency with different phases in below results. We are taking frequency 1 Hz converting it into decimal 2147483 then we converting this into hexadecimal we are getting 0020c49B. In the same way we are converting phase into angle to radian and then converting it into decimal and hexadecimal as well. In this case we are generating the sine wave of above said frequency with $0^o$ phase (simple sine wave) shown in fig 2. In this case we are working on positive edge of clock and reset will be '0'.

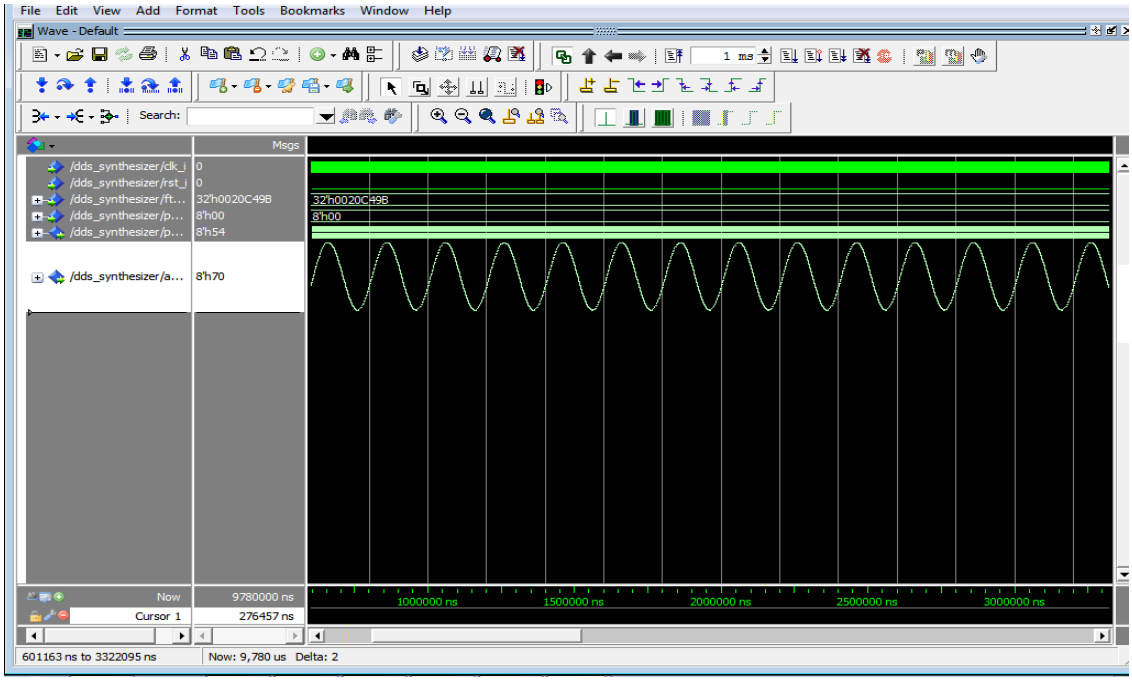


Fig 2: Simulation Results for $0^o$ Phase.

In this case we are generating the sine wave of above said frequency with $90^o$ phase shown in fig 3. In this case we are working on positive edge of clock and reset will be '0'.

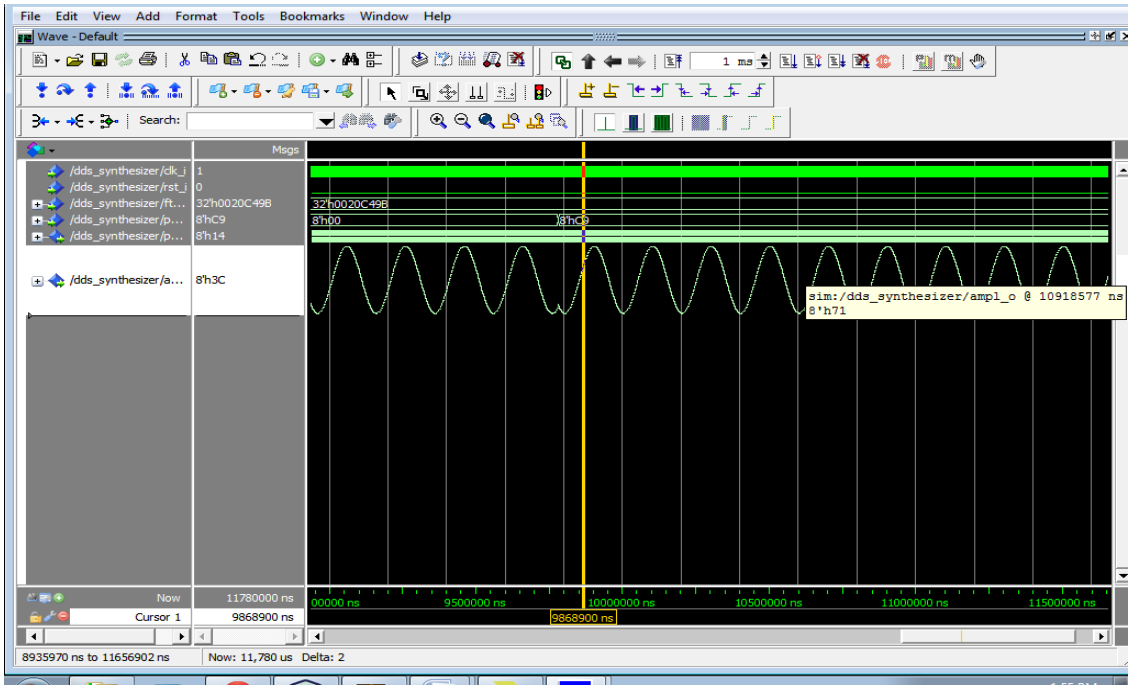


Fig 3: Simulation Results for $90^o$ Phase Shift.

In this case we are generating the sine wave of above said frequency with 45$^{o}$ phase shift. In this case we are working on positive edge of clock and reset will be '0' shown in fig 4.

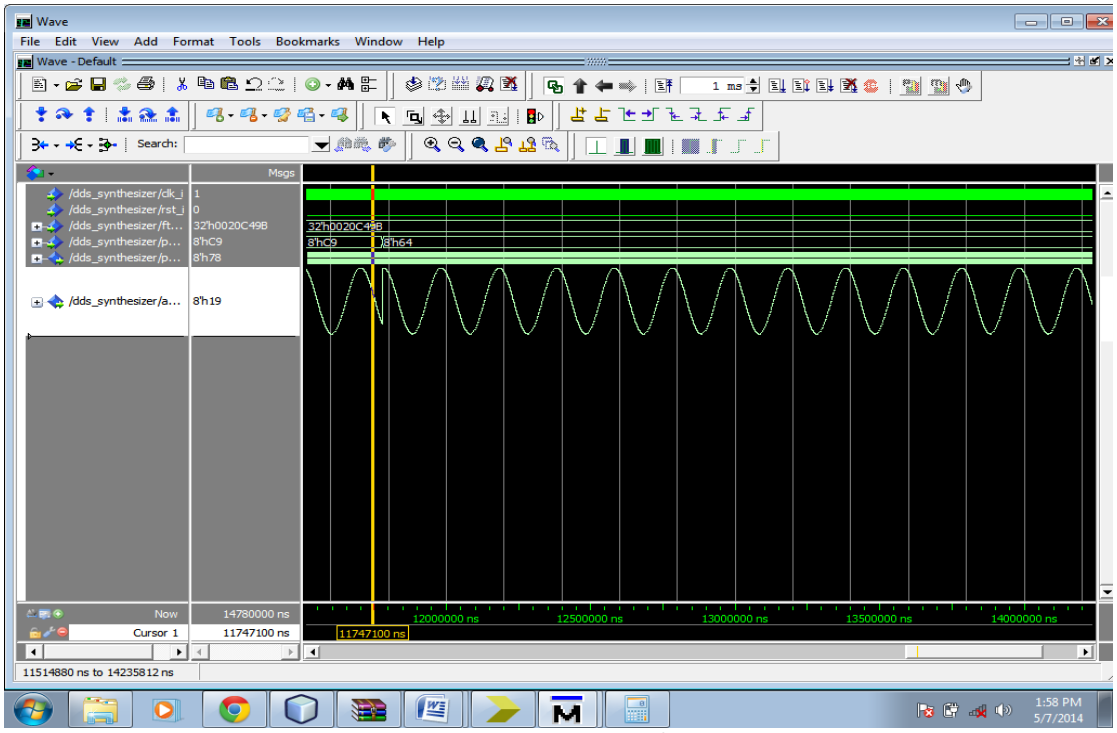


Fig 4: Simulation Results for 45$^{o}$ Phase Shift.

In this case we are generating the sine wave of above said frequency with -12$^{o}$ phase shift. In this case we are working on positive edge of clock and reset will be '0' shown in fig 5.

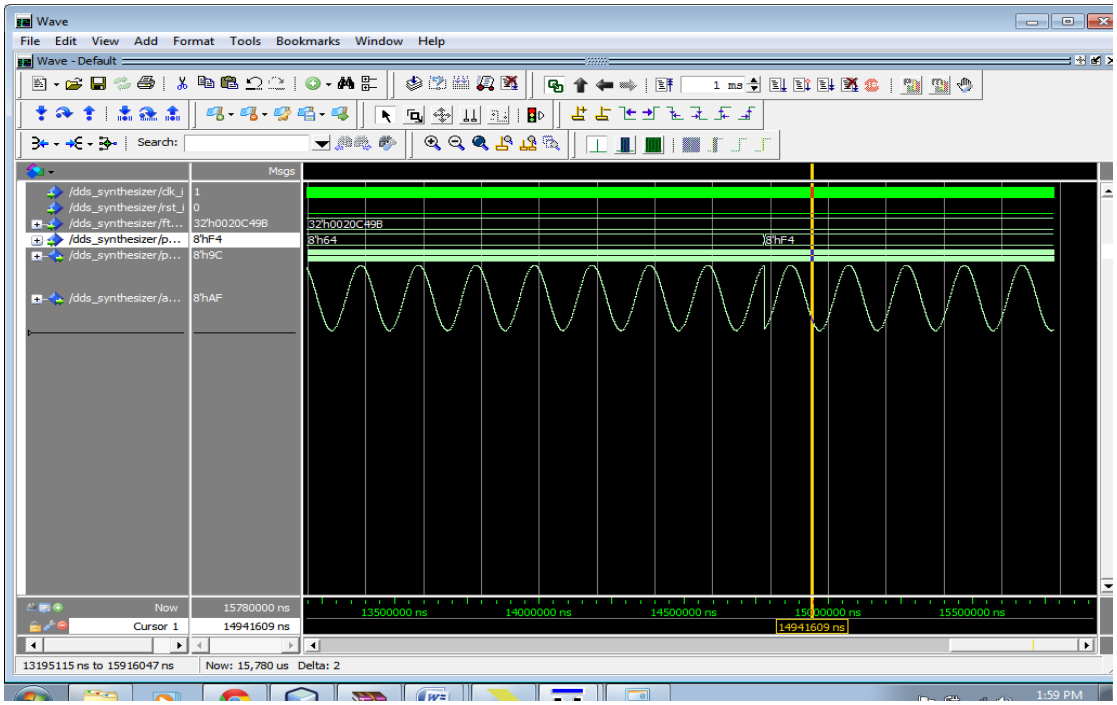


Fig 5: Simulation Results for -12$^{o}$ Phase Shift.

## V. CONCLUSION

The DDS IP core (dds_synthesizer) is a implementation of a direct digital frequency synthesizer (DDS) (also called number controlled oscillator, NCO) which produces a sine wave at the output with a specified frequency and phase (adjustable at runtime). The resolution of the frequency tuning word (FTW), the phase and the amplitude are defined seperately. While the FTW resolution can be set by the generic ftw_width, phase and amplitude resolution are defined as constants phase_width and ampl_width in the seperate package sine_lut_pkg. We have Simulated the Direct Frequency Synthesizer for Sine wave generation from 1Hz to 100 MHz with Amplitude -1V to 1V. The output frequency range / Amplitude range can be change by manipulating the Bit width of Ampl_o or FTW.

We can further enhance our design to generate Triangular/ Square by using the presented design with some more logical gate inserting into it. For implementing on hardware side we must include a DAC.DAC is required to generate the analog pulses as most of the devices supports only analog input.

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