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An Improved Single Phase Transformer less Inverter Topology for Cost Effective PV Systems

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Abstract: *In grid connected PV systems, the elimination of isolation transformer introduces common mode leakage current due to the parasitic capacitance between PV panels and the ground. The common mode leakage current reduces the efficiency of power conversion stage, affects the quality of grid current, deteriorate the electric magnetic compatibility and give rise to various safety threats. In order to eliminate the leakage current, an improved transformer less topology with virtual DC bus concept is proposed here. By connecting the grid neutral line directly to the negative pole of the DC bus, the stray capacitance between the PV panels and the ground is bypassed. The topology consists of only five power switches, two capacitors and the filter section. Therefore, the power electronics cost can be curtailed. This advanced topology can be modulated with the sinusoidal pulse width modulation (SPWM) to reduce the output current ripple. The simulation result of the proposed topology using MATLAB/SIMULINK is presented.*

Keywords: *Common mode leakage current, Transformer less inverter, Unipolar SPWM, Virtual dc bus.*

I. INTRODUCTION

Photovoltaic (PV) power supplied to the utility grid is gaining more and more visibility, while the world's power demand is increasing. . Photovoltaic inverters are widespread in both private and commercial circles. These grid-connected inverters convert the available direct current supplied by the PV panels and feed it into the utility grid.. The grid-connected photovoltaic (PV) systems, especially the low-power single-phase systems, call for high efficiency, small size, light weight, and low-cost grid connected inverters. Most of the commercial PV inverters employ either line-frequency or high-frequency isolation transformers.

However, line-frequency transformers are large and heavy, making the whole system bulky and hard to install. Topologies with high-frequency transformers commonly include several power stages, which increases the system complexity and reduces the system efficiency. Consequently, the transformer less configuration for PV systems is developed to offer the advantages of high efficiency, high power density and low cost.

Unfortunately, there are some safety issues. Without transformer, there is a path for leakage current between PV array and the grid. High frequency common mode voltage generated by inverter appears across stray capacitance formed between the ground and the array terminals. This causes flow of high leakage current from the inverter to the ground. If the leakage current is not regulated within a reasonable margin, it can cause electromagnetic interference, safety issues and grid current distortion. Therefore in order to minimize the leakage current, high frequency common mode voltage must be avoided in transformer less grid connected PV applications.

To avoid the common-mode leakage current, the conventional solution employs the half-bridge inverter or the full-bridge inverter with bipolar sinusoidal pulse width modulation (SPWM), because no variable common-mode voltage is generated. However, the half-bridge inverter requires a high input voltage which is greater than, approximately, 700V for 220-Vac applications. As a result, either large numbers of PV modules in series are involved or a boost dc/dc converter with extremely high-voltage conversion ratio is required as the first power processing stage. The full-bridge inverter just needs half of the input voltage demanded by the half-bridge topology, which is about 350V for 220-Vac applications. But the main drawback is that the full bridge inverter can only employ the bipolar SPWM strategy with two levels, which induces high current ripple, large filter inductor, and low system efficiency. . The main goal of this project is to analyze and model transformer less PV inverter systems with respect to the leakage current phenomenon that can damage the solar panels and pose safety problems.

II. LITERATURE REVIEW

Ideal transformer less inverter generates constant common mode voltage. However, if the voltage varies with time, then a leakage current is produced. For the sake of minimizing this leakage current, different topologies were studied in details.

2.1 Common Mode Current

If the transformer is omitted, the common mode (CM) ground leakage current may appear on the parasitic capacitor between the PV panels and the ground. The existence of the CM current may reduce the power conversion efficiency, increase the grid current distortion, deteriorate the electric magnetic compatibility, and more importantly, give rise to the safety threats. The CM current path in the grid-connected transformer less PV inverter is illustrated in fig 2.1. It is formed by the power switches, filters, ground impedance *Z*G and the parasitic capacitance *C*PV between the PV panels and the ground.

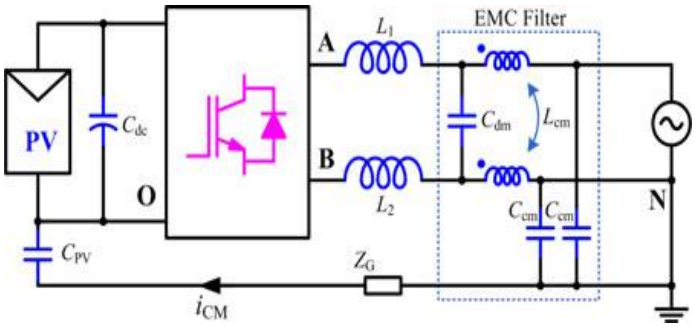


Fig 1. CM current path for the transformer less PV inverters

The simplified equivalent model of the common mode resonant circuit has been derived in as shown in the Figure 2, where CPV is the parasitic capacitor, LA and LB are the filter inductors, icm is the common-mode leakage current.

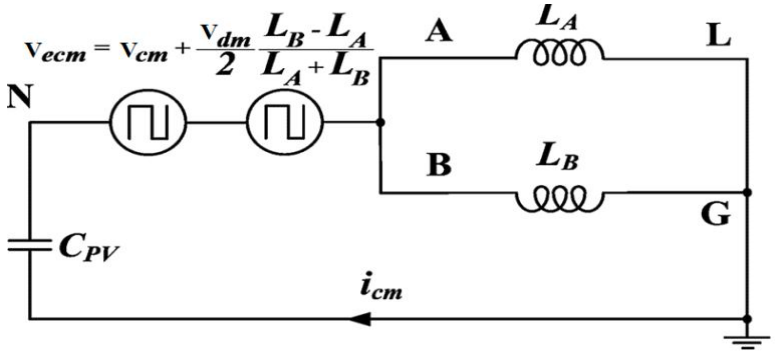


Fig.2 Simplified Equivalent Model of Common-mode Resonant Circuit

An equivalent common-mode voltage Vecm is defined by:

$$V_{ecm} = V_{cm} + \frac{V_{dm}}{2}\frac{L_B - L_A}{L_A + L_B} \qquad (1)$$

where V_{cm} is the common-mode voltage, V_{dm} is the differential mode voltage, V_{AN} and V_{BN} are the output voltages of the inverter relative to the negative terminal N of the dc bus as the common reference.

$$V_{cm} = \frac{V_{AN} + V_{BN}}{2} \qquad (2)$$

$$V_{dm} = V_{AB} = V_{AN} - V_{BN} \qquad (3)$$

It is clear that the common-mode leakage current i_{cm} is excited by the defined equivalent common-mode voltage V_{ecm}.Therefore, the condition of eliminating common-mode leakage current is drawn that the equivalent common-mode voltage V_{ecm} must be kept a constant as follows:

$$V_{ecm} = V_{cm} + \frac{V_{dm}}{2}\frac{L_B - L_A}{L_A + L_B}$$

$$= \frac{V_{AN}+V_{BN}}{2} + \frac{V_{AN}-V_{BN}}{2}\frac{L_B-L_A}{L_A+L_B}$$

=constant (4)

One of the filter inductors LA and LB is commonly zero.The condition of eliminating common-mode leakage current is accordingly met that

$$V_{ecm} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} = V_{AN}$$

=constant ($L_A = 0$) (5)

$$V_{ecm} = \frac{V_{AN} + V_{BN}}{2} - \frac{V_{AN} - V_{BN}}{2} = V_{BN}$$

=constant ($L_B = 0$) (6)

Thus the condition of eliminating leakage current is met such that

$$V_{ecm} = V_{cm} = \frac{V_{AN} + V_{BN}}{2}$$

=constant ($L_A = L_B$) (7)

2.2 Existing Topologies.

2.2.1 Full Bridge topologies

Many solutions have been proposed to realize CM voltage constant in the full-bridge transformerless inverters . A traditional method is to apply the full-bridge inverter with the bipolar sinusoidal pulse width modulation (SPWM). The CM voltage of this inverter is kept constant during all operating modes. Thus, it features excellent leakage currents characteristic. However, the current ripples across the filter inductors and the switching losses are likely to be large. The full-bridge inverters with unipolar SPWM control are attractive due to the excellent differential-mode (DM) characteristics such as smaller inductor current ripple, and higher conversion efficiency. However, the CM voltage of conventional unipolar SPWM full bridge inverter varies at switching frequency, which leads to high leakage currents. The full-bridge inverter with bipolar PWM causes high switching losses and large current ripples and does not eliminate the DC current injected into the grid that has the tendency of saturating the transformer cores. Even though, this topology is being used in some commercial transformerless inverters, it still presents quite low efficiency according to the European standards due to the losses caused by the double switching frequency.

For this reason, some state of the art topologies, such as the H5 inverter, the Heric inverter etc. have been developed based on full bridge inverter, to keep Vcm constant when unipolar modulation is used.

H5 circuit

This topology is based on the full bridge with an extra switch on the DC side. In this topology, the upper switches operate at grid frequency while the lower switches operate at high frequency . The extra switch operates at high frequency and guarantees the disconnection of the DC source from the grid. This topology has two main disadvantages. The first one is the high conduction losses due to the fact that three switches operate simultaneously. The second one is that the reactive power flow is not possible due to the control strategy.

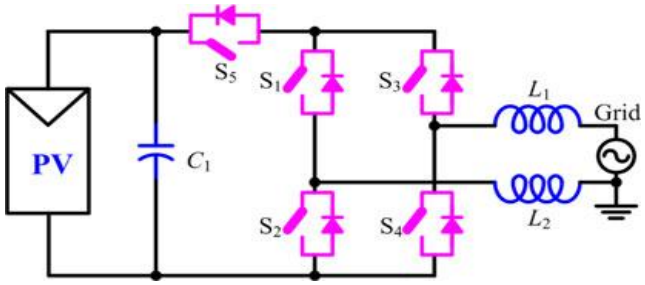


Fig 3. H5 circuit

The H-5 topology, that uses a full-bridge consisting of the four switches S1, S2, S3 and S4, and the DC-bypass S5 switch. The switches S1 and S2 are operated at grid frequency, whereas S3, S4 and S5 are operated at high frequency. During current free-wheeling period, S5 is open, disconnecting PV panels from the inverter full H-bridge. The free-wheeling path is closed by the transistor S1 and the inverse diode of S3 for the positive half-cycle of the electrical grid, and by the transistor S3 and the inverse diode of S1 for the negative half-cycle

Heric converter:

HERIC (Highly Efficient and Reliable Inverter Concept) topology is another structure that avoids a fluctuating potential on the DC terminals of the PV generators by means of disconnecting the converter from the grid.

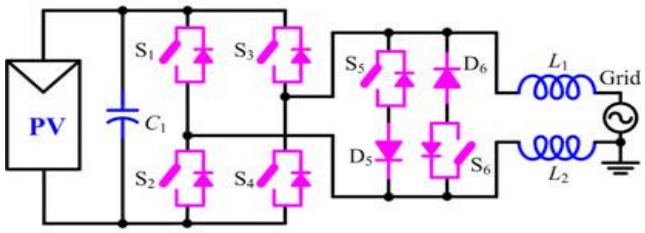


Fig 4. Heric converter

It combines the advantages of the unipolar and bipolar modulations. It has a three level output voltage, a high efficiency and a low leakage current. However, the HERIC topology presents low frequency harmonics and does not allow for reactive power flow. This is due to the control strategy.

2.2.2 Half bridge inverter topologies.

In half-bridge inverter the grid neutral line directly connected to the midpoint of the dc bus. In this way, the voltage across the parasitic capacitor is clamped to be constant by the dc bus capacitor. However, this method has an important disadvantage that the required dc bus voltage should be doubled compared with the full-bridge topologies. For the 220 Vac system, it can be as high as 700 V. Although the three-level neutral point clamped (NPC) circuit can help improve the performance of the half-bridge inverter, the dc bus voltage is still high. The half bridge inverter requires a high input voltage and a boost converter in the DC side that would increase the inverter size and cost and reduce its efficiency down to 92% For this reason the half bridge is not recommended.

Conventional half bridge inverter:

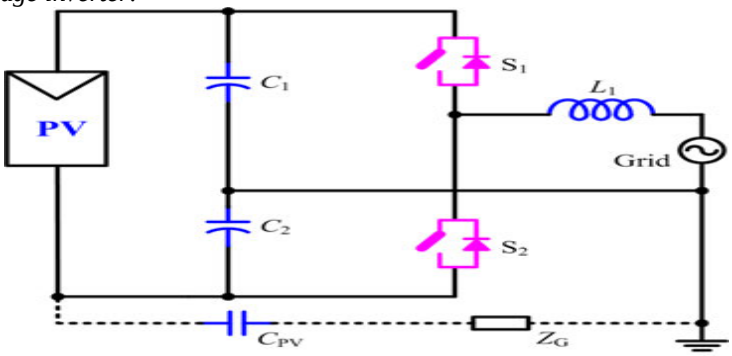


Fig 5.Conventional half bridge inverter

Firstly, with only two switches in series, the half bridge converter is only capable of transmitting a pulse train to the output with a magnitude of half that of the full bridge . This means that for the same DC input voltage a half bridge converter may require a front end boost converter to step up the input voltage of the inverter. Introducing a new stage of the inverter will introduce charging and power devices which will result in additional losses and an overall lower efficiency. As a higher DC input to the half bridge converter is required, it also means implemented switching device with a higher voltage rating. Such switching devices typically have higher losses and must be switched at a slower rate which may result in an increase in harmonic content of the output. It is also worth noting that the topology is only capable of implementing bipolar switching as the design consists of two switches making a freewheeling period impossible

Another associated advantage of utilizing a half bridge topology is that the design naturally prevents DC current injection into the AC network . As a half bridge converter implements a split input capacitance, one capacitor is always present in the current conducting path.

Neutral point clamped half bridge inverter:

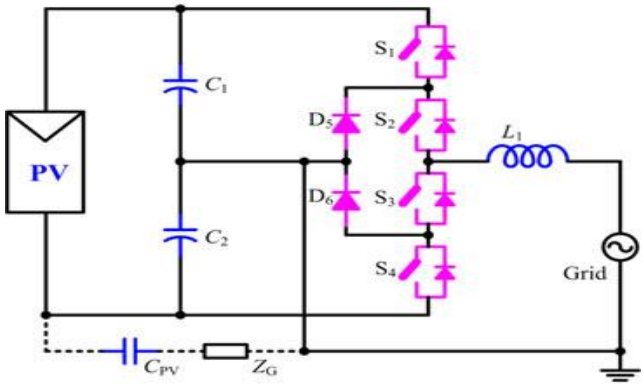


Fig 6.Neutral point clamped half bridge inverter

Although the Neutral-Point-Clamped (NPC) inverter can be considered a mature solution in traction applications, it has only been recently applied in PV systems. It shares most of the advantages of the previously presented circuits, namely, no internal reactive-power flow, output voltage with three levels, and minimized voltage oscillations of the PV array to ground. A serious drawback for the single-phase application is the requirement for a high input-voltage level; the double in comparison with the previous circuits. Another critical point regarding the application of such circuit in grid-connected appliances is the higher transient voltage across the middle switches.

2.2.3 Other topologies:Karschny inverter topology

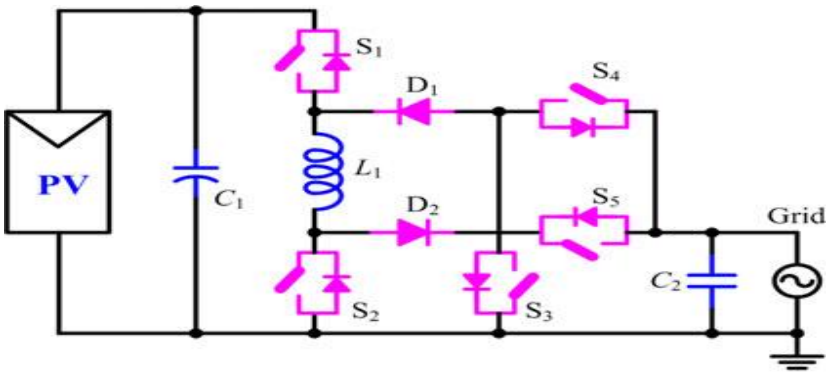


Fig 7. Karschny inverter topology

The basic topology allows a direct connection between the output neutral and the negative terminal of the PV array, eliminating any voltage oscillations and, in addition, allowing the operation with special thin-film panels. The basic structure here consists of a circuit capable of operating as a buck and boost stage with auxiliary switches defining the output polarity. The large amount of semiconductors in the current path and the necessity of storing the whole energy in the inductor lead, respectively, to high amount of losses and higher construction cost and size.

III. PROPOSED TOPOLOGY

Here ,a novel topology generation strategy called the virtual dc bus concept is proposed for the transformer less grid connected pv inverter. In this solution, the grid neutral line is connected directly to the negative pole of the dc bus, so that voltage across the parasitic capacitor is clamped to zero. As a result, the CM current is eliminated completely.Mean while,the virtual dc bus is created to help generate the negative output voltage. The required dc bus voltage is still the same as the full bridge, and there is not any limitation on the modulation strategy since the CM current is removed naturally by the circuit structure. In this way, the advantage of the full bridge and half bridge based solutions are combined together.

3.1 Virtual DC Bus Concept

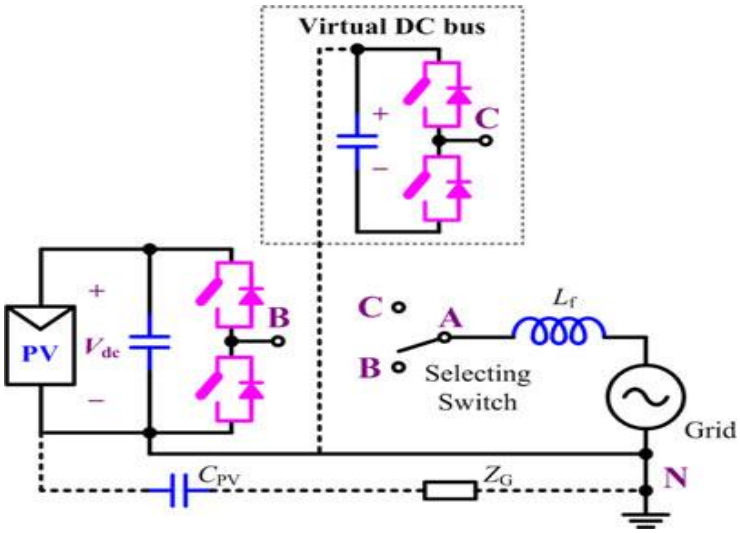


Fig 8.Virtual dc bus concept

By connecting the grid neutral line directly to the negative pole of the PV panel, the voltage across the parasitic capacitance *C*pv is clamped to zero. This prevents any leakage current flowing through it. With respect to the ground point N, the voltage at midpoint B is either zero or +*V*dc, according to the state of the switch bridge. The purpose of introducing virtual DC bus is to generate the negative output voltage, which is necessary for the operation of the inverter. If a proper method is designed to transfer the energy between the real bus and the virtual bus, the voltage across the virtual bus can be kept the same as the real one. The positive pole of the virtual bus is connected to the ground point N, so that the voltage at the midpoint C is either zero or −*V*dc.

The dotted line in the figure indicates that this connection may be realized directly by a wire or indirectly by a power switch. With points B and C joined together by a smart selecting switch, the voltage at point A can be of three different voltage levels, namely +*V*dc, zero and –*V*dc. Since the CM current is eliminated naturally by the structure of the circuit, there's not any limitation on the modulation strategy, which means that the advanced modulation technologies such as the unipolar SPWM or the double frequency SPWM can be used to satisfy various PV applications

3.2 Derived Topology And Modulation Strategy.

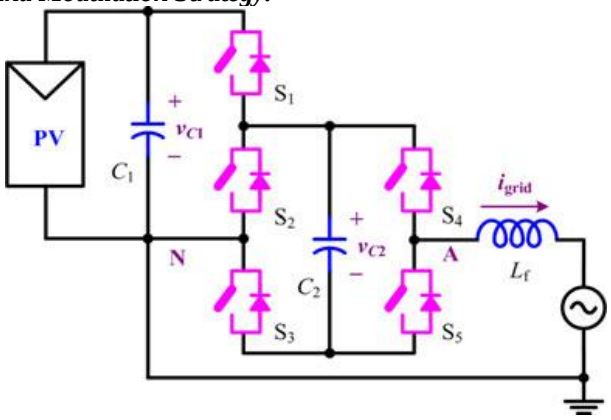


Fig 9. Proposed topology

Based on the negative voltage generation concept, an inverter topology is derived to show the clear advantages of the proposed methodology. It consists of five power switches S1~S5 and only one single filter inductor *L*f. The PV panels and capacitor *C*1 form the real DC bus while the virtual DC bus is provided by *C*2. With the switched capacitor technology, *C*2 is charged by the real DC bus through S1 and S3 to maintain a constant voltage. This topology can be modulated with the unipolar SPWM and double frequency SPWM

3.3 Unipolar SPWM

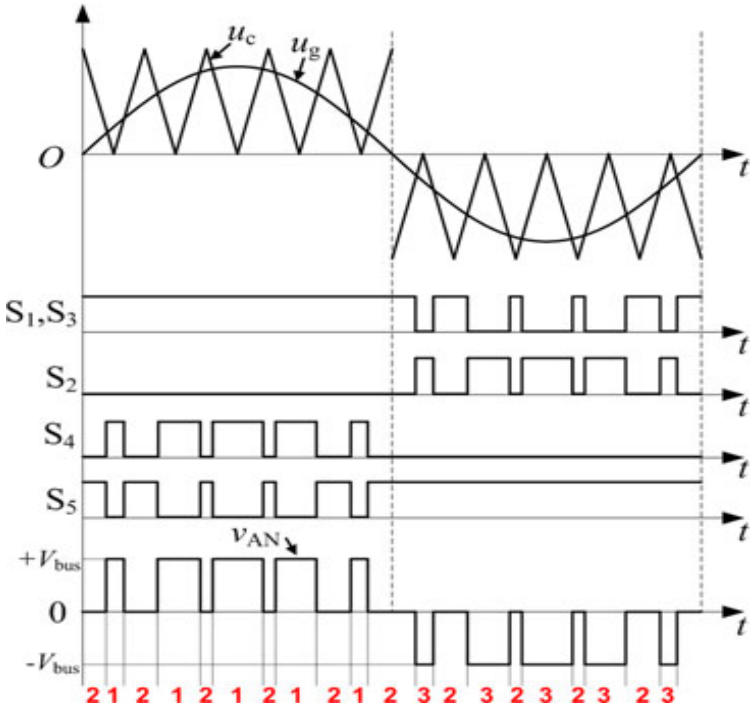
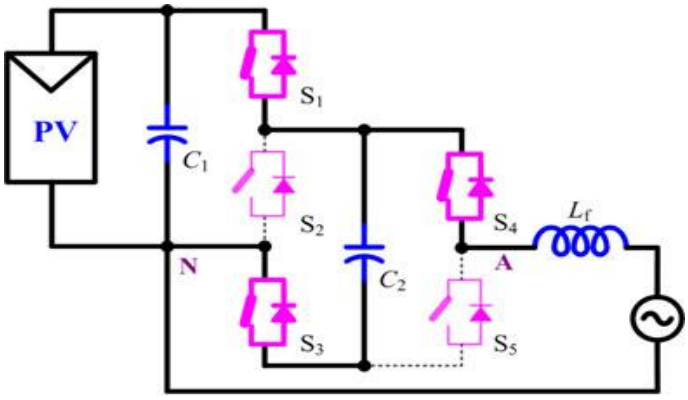


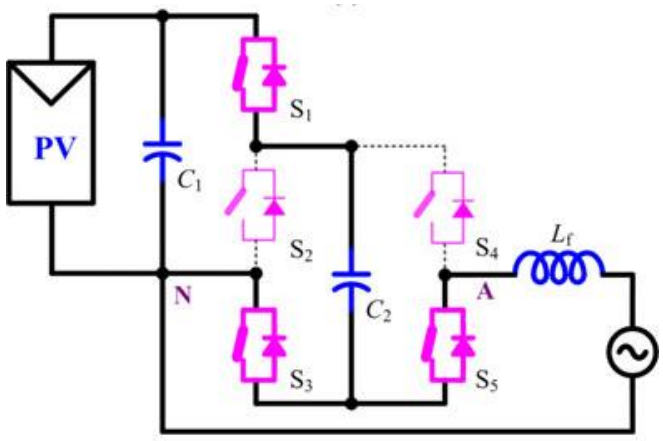
Fig 7 Unipolar SPWM for proposed topology

The gate drive signals for the power switches are generated according to the relative value of the modulation wave *u*g and the carrier wave *u*c. During the positive half grid cycle,*u*g> 0. S1 and S3 are turned on and S2 is turned off, while S4 and S5 commutate complementally with the carrier frequency. The capacitors *C*1 and *C*2 are in parallel and the circuit rotates between state 1 and state 2 . During the negative half cycle, *u*g< 0. S5 is turned on and S4 is turned off. S1 and S3 commutate with the carrier frequency synchronously and S2 commutates in complement to them. The circuit rotates between state 3 and state 2. At state 3, S1 and S3 are turned off while S2 is turned on. The negative voltage is generated by the virtual DC bus *C*2 and the inverter output is at negative voltage level. At state 2, S1 and S3 are turned on while S2 is turned off. The inverter output voltage VAN equals zero, meanwhile *C*2 is charged by the DC bus through S1 and S3.

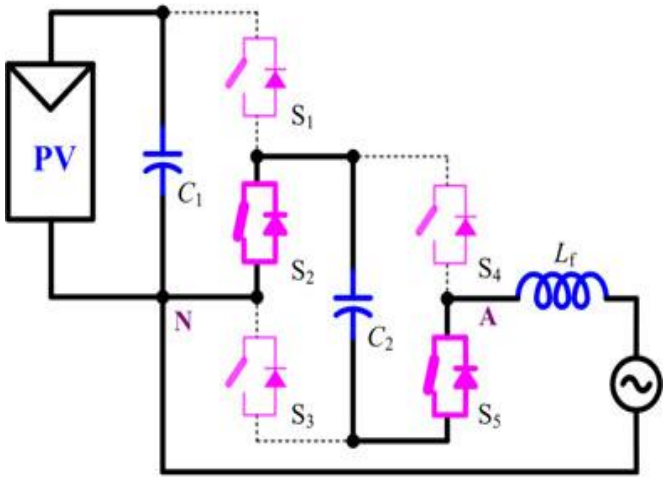
3.4 Operating States for Proposed Topology



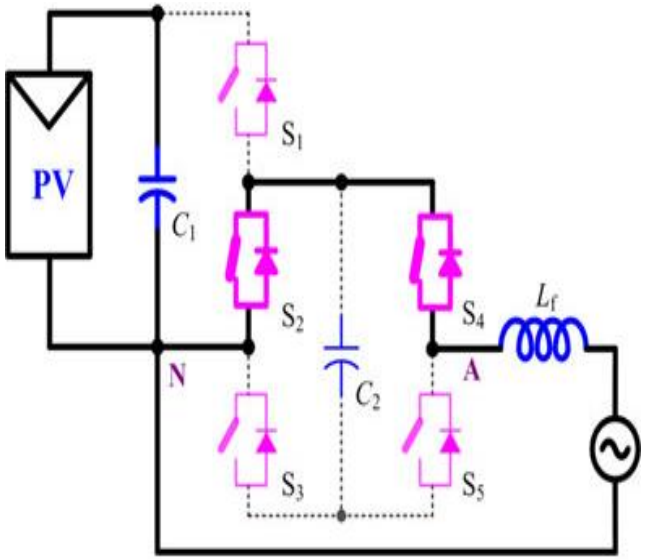
(a) State 1



(b) State 2



c) State 3



(d) State 4

Fig 10.Operating States of Proposed Topology

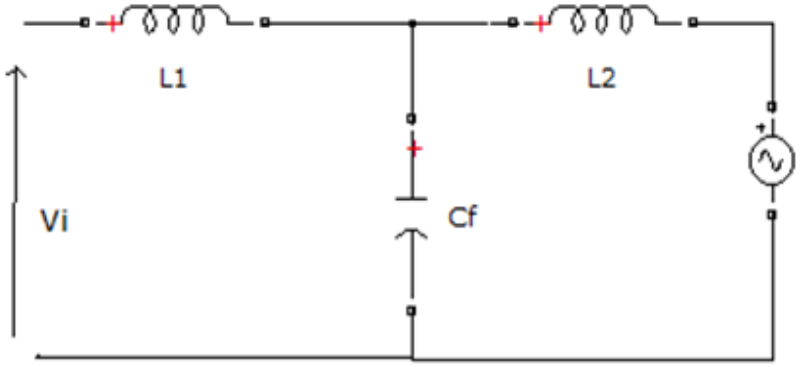
For all of the four operation states, there is no limitation on the direction of the output current *i*grid, since the power switches with anti parallel diodes can achieve bidirectional current flow. Therefore, the proposed topology has the capability of feeding reactive power into the grid to help support the stability of the power system.

The proposed topology is also immune against transient overvoltage of the grid. During the mains positive voltage spikes, the voltage at point A is clamped at *V*dc by *C*1 and the anti parallel diodes of S1 and S4 . Similarly, during the negative voltage spikes, the voltage at point A is clamped at −*V*dc by *C*2 and the anti parallel diodes of S2 and S5 . Therefore, the mains transient overvoltage does not pose a safety threat for the inverter.

IV. SYSTEM DESIGN CONSIDERATIONS

A 500 W prototype is considered to verify the functionality of the proposed topology and the idea of virtual dc bus concept. The terminal voltage for a 500 W PV panel is typically 40-60 V. Here a 400 V dc bus is considered. The LCL filter is used to reduce the output current ripple. The grid voltage is 220Vac and frequency is 50 Hz. MOSFET switches are employed as power switches.

4.1 Design Of LCL Filter



A LCL filter is often used to interconnect an inverter to the utility grid in order to filter the harmonics produced by the inverter.The LCL filter achieves a higher attenuation along with cost savings, given the overall weight and size reduction of the components.

L_1: inverter side inductor

L_2: grid side inductor

C_f: filter capacitor.

P_n:be the rated active power.

V_{ph}:phase voltage.

V_{dc}:dc link voltage.

f_g:grid frequency.

f_{sw}:switching frequency

E_n:rms grid voltage

$k_a = attenuation\ factor$

Assume 10% ripple in rated current

$* \Delta I_l \max = 0.1\ Imax$ …… (8)

$* Imax = \frac{P_n\sqrt{2}}{V_{ph}}$ …….. (9)

$$Imax = \frac{500 * \sqrt{2}}{220} = 3.214$$

From equation (1)

$\Delta I_l \max = 0.1\ Imax$ =0.1*3.214 =0.3214

$L_1 = \frac{V_{dc}}{6 f_{sw} \Delta I_l max}$ …… (10)

$$L_1 = \frac{400}{6 * 20000 * 0.3214} = 10.37\ mH$$

The base impedance and base capacitance are defined by:

$$Z_b = \frac{En^2}{P_n} \quad \text{(11)}$$

$$= \frac{220^2}{500} = 96.8$$

$$C_b = \frac{1}{\omega_g Z_b} \quad \text{(12)}$$

$$= \frac{1}{2\pi * 50 * 96.8} = 3.288 \times 10^{-5}$$

For the design of the filter capacitance, it is considered that the maximum power factor variation seen by the grid is 5%,indicating that the base impedance of the system is adjusted as follows:

$$C_f = 0.05 C_b \quad \text{(13)}$$

C_f =1.64×10^{-6} F.

Set desired attenuation factor k_a=20%=0.2

Switching frequency f_{sw} =20 kHz.

$$L_2 = \frac{\sqrt{(\frac{1}{k_a}^2 + 1)}}{C_f f_{sw}^{\ 2}} \quad \text{(14)}$$

=7.77mH.

4.2 Design Of dc Capacitors

$$C_1 = \frac{p}{2.\omega_{grid}\ U_c \Delta V_{c1}} \quad \text{(15)}$$

U_c:mean voltage across capacitor

$\Delta V_{c1} = 4.23\ V$

C_1=470µF

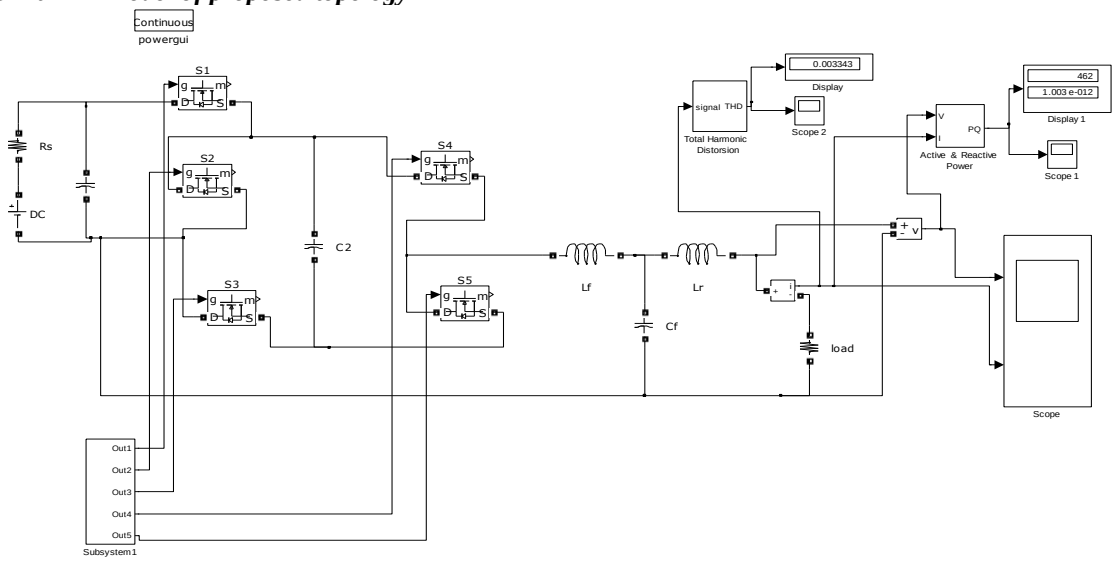
$\Delta V_{c2} = 2.11\ V$

$$C_2 = \frac{p}{2.\omega_{grid}\ U_c \Delta V_{c2}} \quad \text{(16)}$$

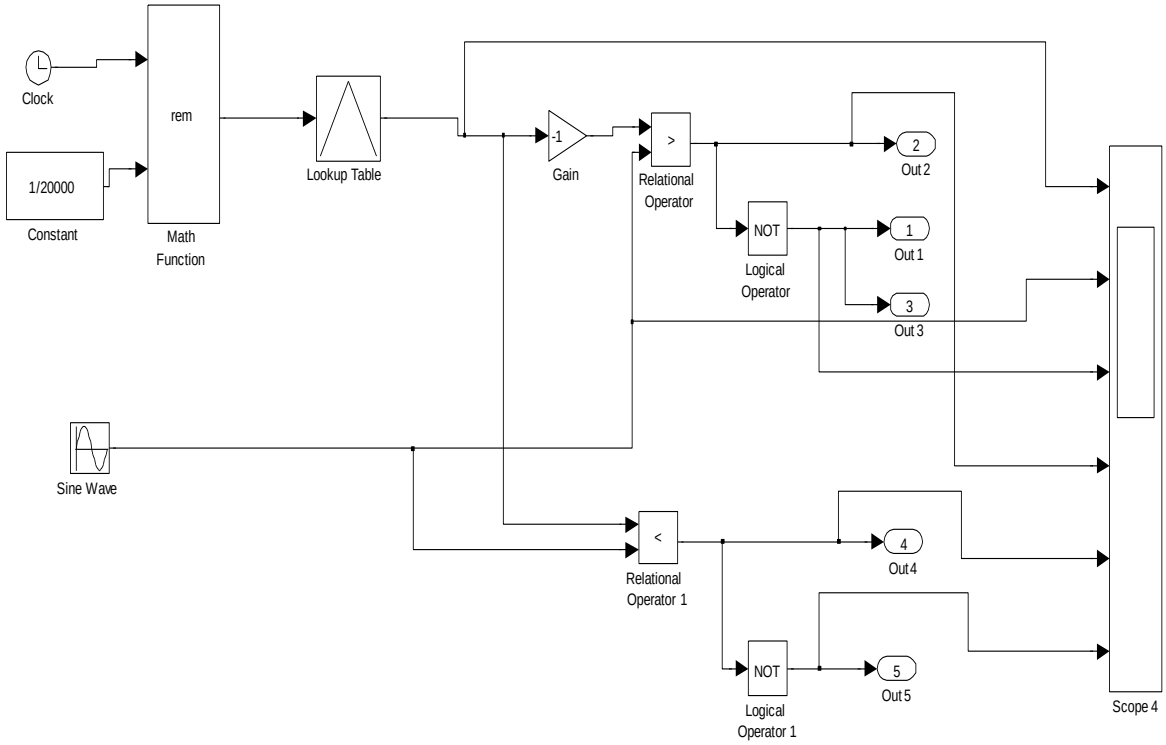
C_2= 940µF.

V. EXPERIMENTAL RESULTS

5.1 Simulink model of proposed topology

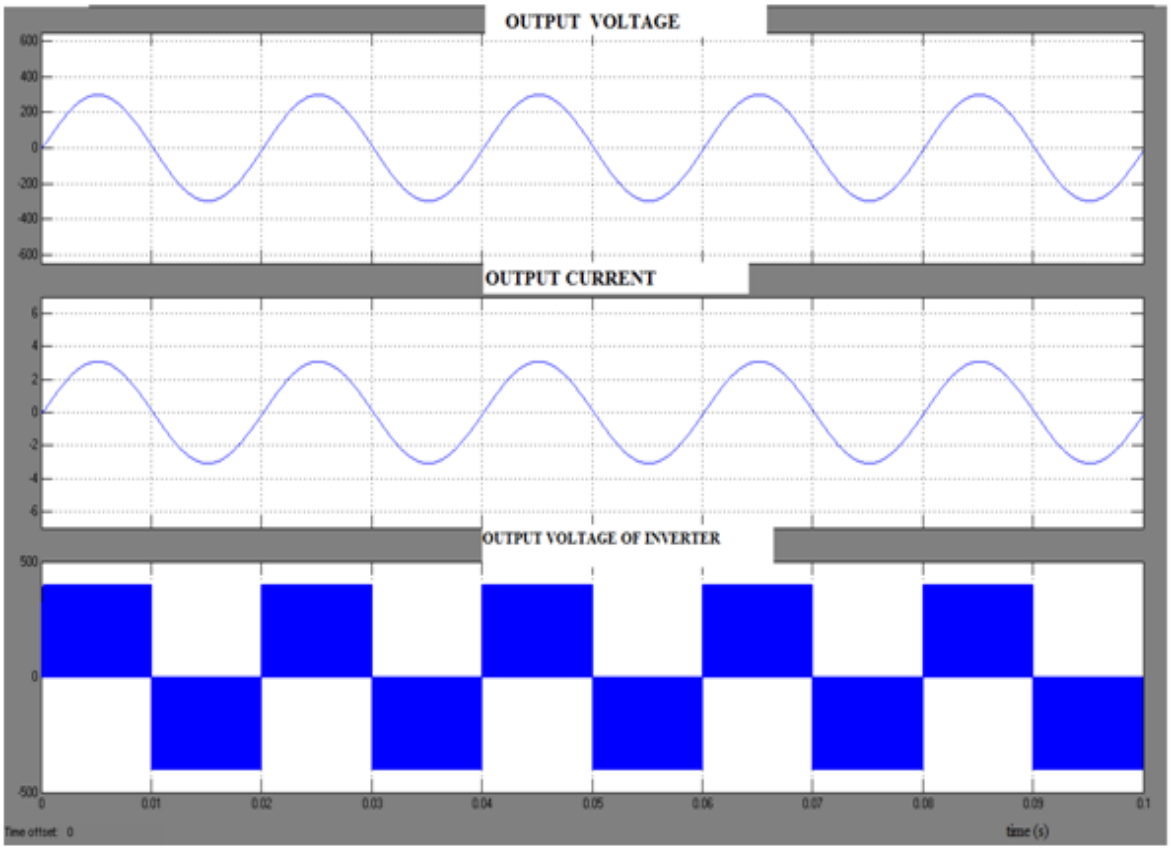


5.2 Simulink model for unipolar SPWM

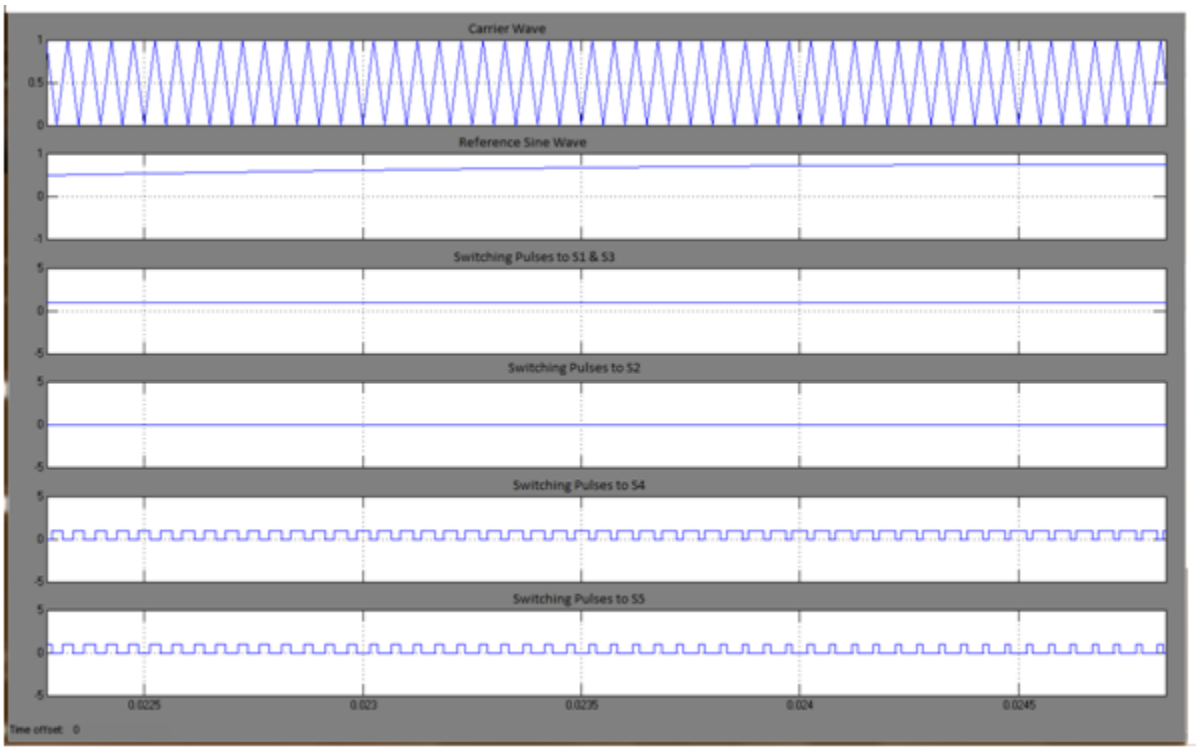


5.3 Simulation Results

5.3.1 output waveforms



5.3.2 switching pulses



VI. Conclusion

The concept of the virtual DC bus is proposed to solve the CM current problem for the transformer less grid-connected PV inverter. By connecting the negative pole of the DC bus directly to the grid neutral line, the voltage on the stray PV capacitor is clamped to zero. This eliminates the CM current completely. Meanwhile, a virtual DC bus is created to provide the negative voltage level. The required DC voltage is only half of the half bridge solution, while the performance in eliminating the CM current is better than the full bridge based inverters. Based on this idea, a novel inverter topology is proposed with the virtual DC bus concept by adopting the switched capacitor technology. It consists of only five power switches and filter circuit. The proposed topology is especially suitable for the small power single phase applications, where the output current is relatively small so that the extra current stress caused by the switched capacitor does not cause serious reliability problem for the power devices and capacitors. With excellent performance in eliminating the CM current, the virtual DC bus concept provides a promising solution for the transformer less grid-connected PV inverters. The software tool used in this project is MATLAB 2007b.

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