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Design of Multiplier Less 32 Tap FIR Filter using VHDL

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Abstract: *This Paper provide the principles of Distributed Arithmetic, and introduce it into the FIR filters design, and then presents a 32-Tap FIR low-pass filter using Distributed Arithmetic, which save considerable MAC blocks to decrease the circuit scale and pipeline structure is also used to increase the system speed. The implementation of FIR filters on FPGA based on traditional method costs considerable hardware resources, which goes against the decrease of circuit scale and the increase of system speed.*
It is very well known that the FIR filter consists of Delay elements, Multipliers and Adders. Because of usage of Multipliers in early design gives rise to 2 demerits that are:
(i) Increase in Area and
(ii) Increase in the Delay which ultimately results in low performance (Less speed).
So the Distributed Arithmetic for FIR Filter design and Implementation is provided in this work to solve this problem. Distributed Arithmetic structure is used to increase the recourse usage and pipeline structure is used to increase the system speed. Distributed Arithmetic can save considerable hardware resources through using LUT to take the place of MAC units

Keywords: *Distributed Algorithm, FIR Filter, Modelsim 10.2a, VHDL, Xilinx ISE 14.2.*

I. Introduction

For many decades the aim of developing new hardware was to make devices smaller and faster. The amount of power they consumed was hardly an issue, since the power wasn't the bottle neck. Today we face a different situation, as the demand for real time application with a long battery lifetime is increasing.

Today, design of low power signal processing circuits is an important part of the electronics industry. This is because portable computing and communication devices like cellular phones and laptop computers have become very popular. The development seems to take a turn towards wireless communication and flexibility in the sense that a stationary port is unnecessary. This challenges the industry to produce low power devices and it challenges researchers to find new, less power consuming algorithms for the processes carried out by portable devices. An important process is the digital signal processing (DSP). DSP is the transference of data between devices, such as cellular phone communication, wireless Internet usage and digital TV transmission to mention a few. Finite impulse response (FIR) filtering is a central task in DSP. By reducing the power needed to process data through such a filter, power can be significantly reduced.

In signal processing, the function of a filter is to remove unwanted parts of the signal, such as random noise, or to extract useful parts of the signal, such as the components lying within a certain frequency range [2].

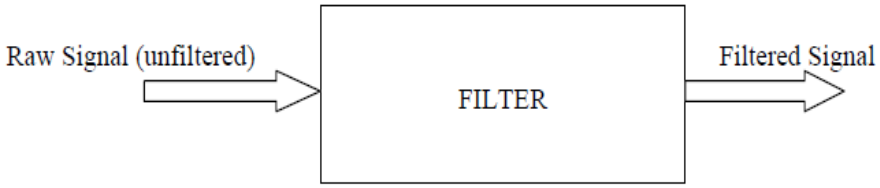

Fig 1: A block diagram of a basic filter.

A filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Ideally, a filter will not add new frequencies to the input signal, nor will it change the component frequencies of that signal, but it will change the relative amplitudes of the various frequency components and/or their phase relationships. Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject signals in other frequency ranges.

There are two types of filter: analog and digital. FIR Filter is the kind of digital filter, which can be used to perform all kinds of filtering.

II. Related Work

A Ruan,A.W., Liao,Y.B., Li,P. , Li,J.X., (2009) [4] proposed and presented An ALU based universal FIR filter where various FIR filters can be implemented just by programming instructions in the ROM with identical hardware architecture. They presented Arithmetic Logic Unit (ALU) based universal FIR filter suitable for implementation in Field Programmable Gate Arrays (FPGA) is proposed in this paper. Multiplier and accumulator based architecture used in conventional FIR, the proposed ALU architecture implements FIR functions by using accumulators and shift-registers controlled by the instructions of ROM.

Nekoei,F., Kavian,Y.S., Strobel,O., (2010) [5] presented realization of digital FIR filters on field programmable gate array devices was proposed. Two common architectures called direct and transposed architectures were employed for implementing FIR filters on a Xilinx SPARTAN2-XC2S50-5I-tq144 FPGA using Verilog hardware description language codes.

X.Jiang, Y.Bao(2010) proposed a structure characteristics and the basic principles of the finite impulse response (FIR) digital filter, and gives an efficient FIR filter design based on FPGA. Use MATLAB FDATool to determine filter coefficients, and designed a 16-order constant coefficient FIR filter by VHDL language, take use of Quartus-2 to simulate filters, the results meet performance requirements.

Li,J., Zhao,M., Wang,X., (2011) [6] They used distributed algorithm and its several structures, an implementation method of 60-order FIR filter based on FPGA is presented, which converts multiplication to look-up table structure, and implement multiplication operation. They used FPGA as the hardware platform. This filter system has a good performance, the filter speed is higher and the resource occupation is fewer.

Beyrouthy,T., Fesquet,L., (2011) [3] presented an asynchronous FIR Filter architecture was presented, along with an asynchronous Analog to digital converter(A-ADC). They designed FIR Filter architecture using the micro-pipeline asynchronous style. They successfully implemented for the first time on a commercial FPGA board (Altera-DE1). A specific library has also been designed for this purpose. It allows the synthesis of asynchronous primitive blocks (the control path in this case) on the synchronous FPGA. Simulation results of the FIR Filter after place and route validate the implementation. This work is still going on, in order to optimize the implementation.

III. Methodology

3.1 Multiplierless FIR Filter:

It is widely accepted that the multiplication is the main source of complexity in a FIR filter. In other words the multiplication consumes most area and is the main source of delaying the throughput, in addition to its high consume of power. An array multiplier of length L consumes an area $O(L^2)$, whereas an adder spreads over only O(L) area [1]. The multiplication by a constant can be represented behaviorally as in figure 2.

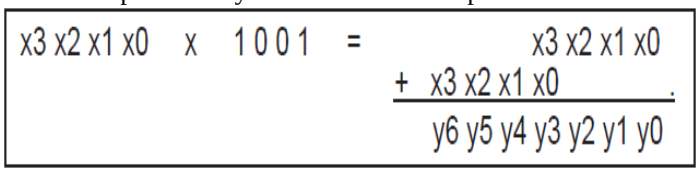

Fig 2: Multiplication using reduced additions

3.2 Distributed Arithmetic algorithms:

In multiplierless architectures the replacement of the multiplier with a series of additions and shifts is on the cost of speed. The Distributed Arithmetic (DA) is a bit-serial computation process that offers speeds approaching the original array multiplier's speed, and at the same time keeping the power consumption down on the same level as the competing dedicated hardware and ASIC's power consumption. [7].

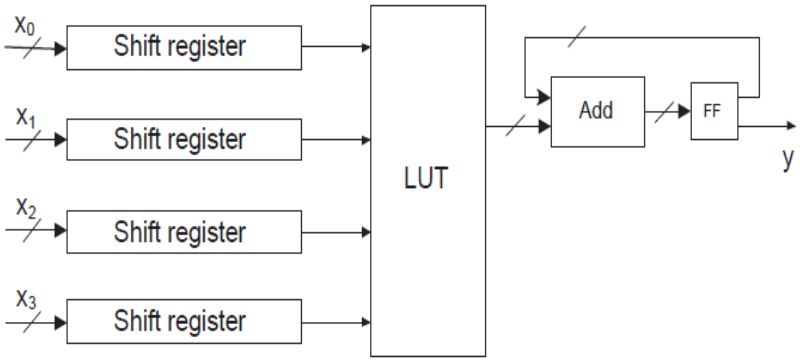

Fig 3: Distributed Arithmetic, the principle

The DA standard architecture is shown in figure 3. The variables are fed into the shift-registers. From there, one by one they are fed into the Look Up Table (LUT). The LUT is the replacement of a multiplication, since it consists of precomputed data.

3.3 Architecture implementation in VHDL:

The architectures implemented by the Distributed Arithmetic. The design grows in size according to the number of taps used. An 8 tap implementation is illustrated in figure 4. We will design 32 tap multiplier less Fir Filter.

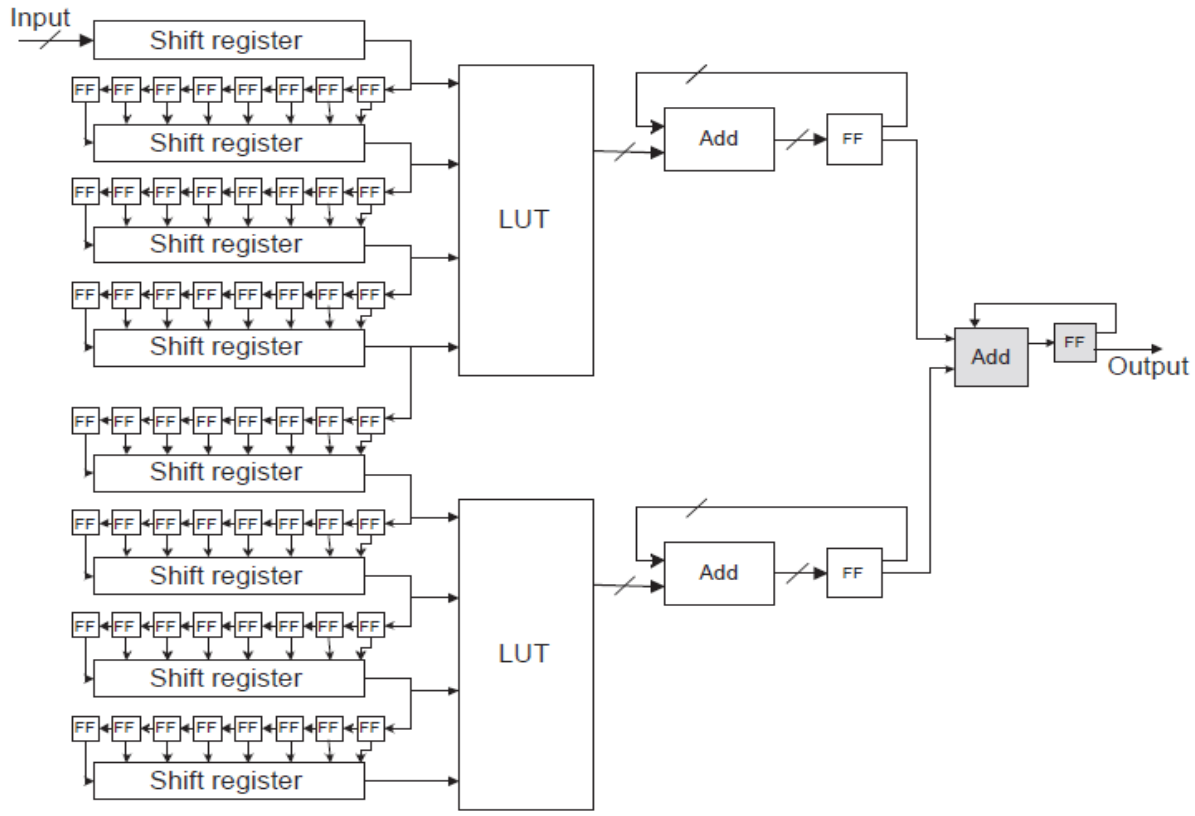

Fig 4: 8 tap binary FIR Filter implementation

IV. Simulation Results

In this paper we designed the low pass FIR filter for sampling frequency 48 KHz to meet the given specification (i.e.: Pass band edge: 9.6 KHz, Stop band Edge:12KHz, Pass band Edge:1 dB and Stop band Attenuation. : 90dB).The implementation of highly efficient serial DA algorithm was presented in this work. Simulation results are shown below for different sample inputs in 16 bit hexadecimal values and the output is shown in time domain. In fig 5 shows filtered output for sample value 1234h.

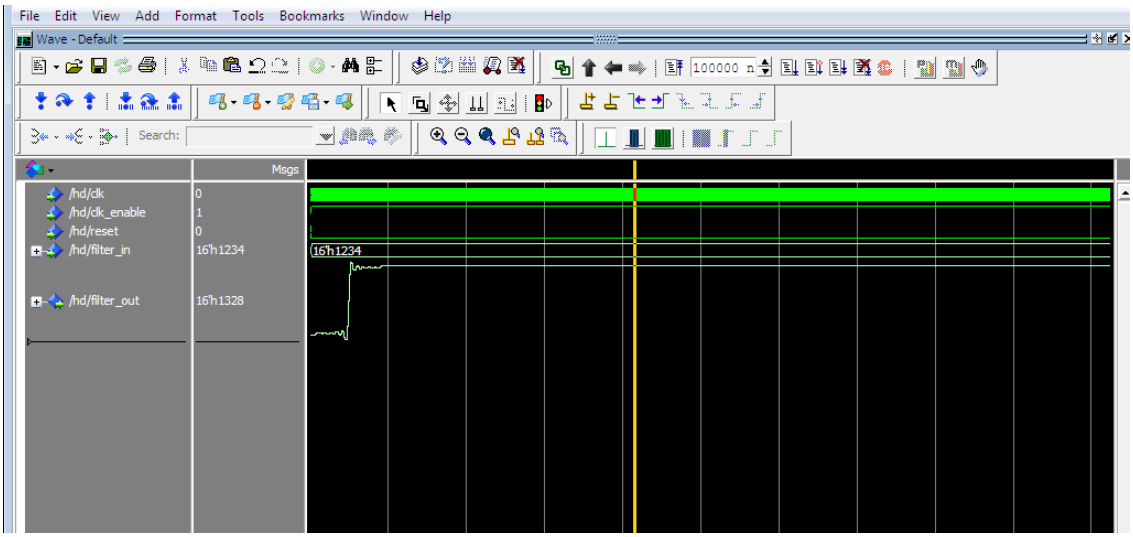

Fig 5: Simulation Result for 1234h.

In fig 6 shows filtered output for sample value 0123h.

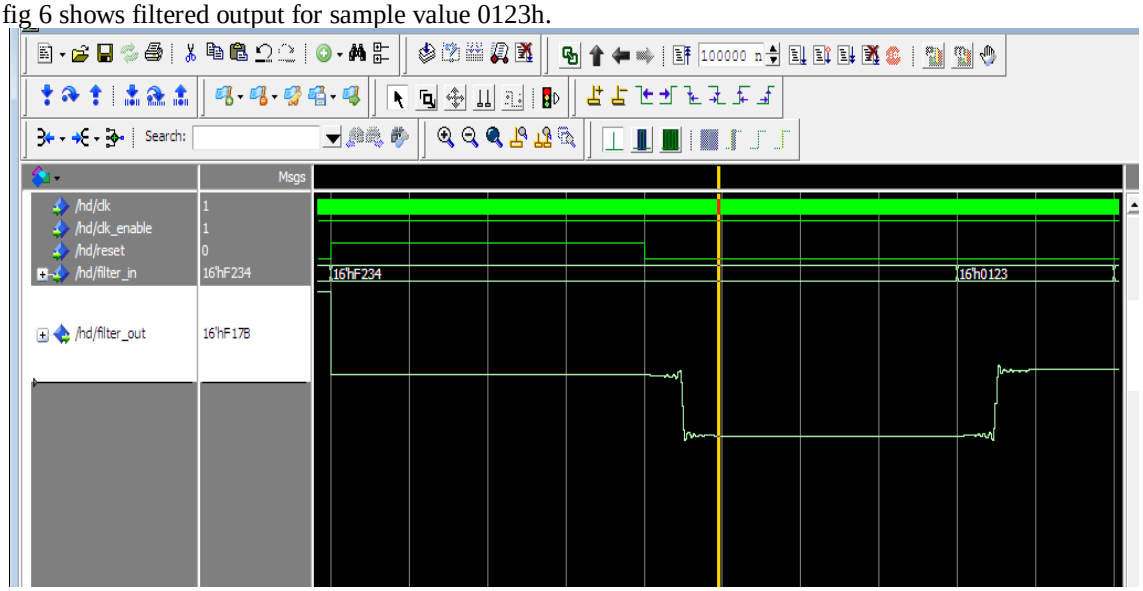

Fig 6: Simulation Result 0123h.

We are using Xilinx tool for synthesis our code fig 7 shows the main RTL of our code and fig 8 shows the internal RTL of our code.

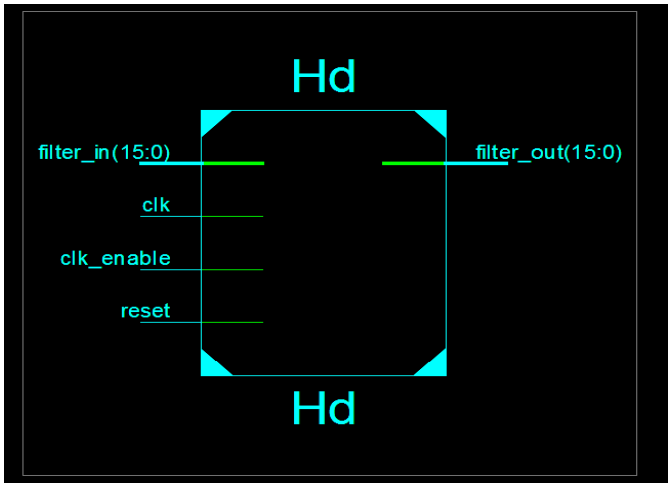

Fig 7: Main RTL

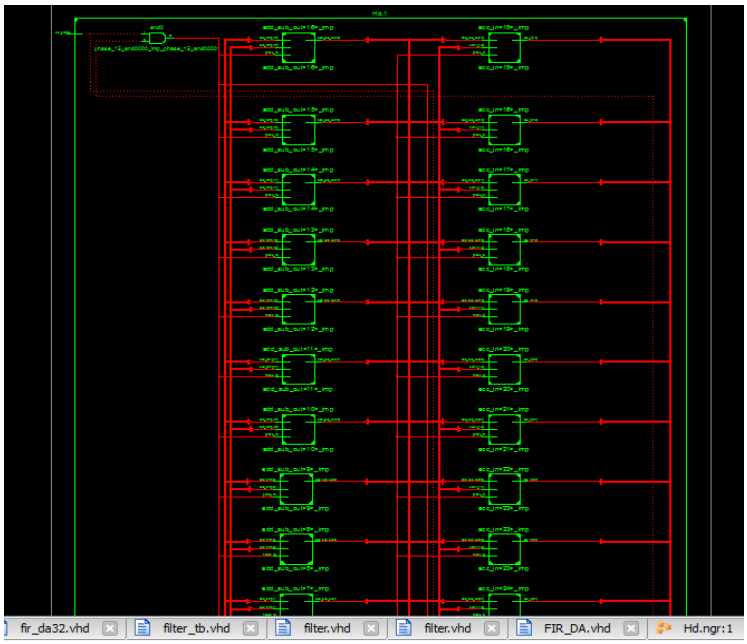

Fig 8: Internal RTL

V. Conclusion

We designed a double-precision low pass direct form FIR filter with Sampling Frequency 48KHZ to meet the given specification(i.e.: Pass band edge: 9.6KHz, Stop band Edge:12KHz, Pass band Edge:1 dB and Stop band Attenuation 90dB).The implementation of highly efficient serial DA algorithm was presented in this work. The results were analyzed for 32-tap FIR filter using partitioned input based LUT on Xilinx 8.2 as a target of SPARTAN-3E FPGA device .The speed performance of the Parallel DA FIR Filter was superior in comparison to all other techniques . In 32 tap FIR filter, speed of parallel DA FIR design technique become 3 times faster than that of conventional FIR filter. The proposed algorithm for FIR filters is also area efficient since approximately 50% of the area is saved with this technique as compared to conventional FIR filter design. Area efficiency and high speed is achieved with parallel DA technique at very slight cost of power consumption for large tap FIR filter. Since, distributed arithmetic FIR filters are area efficient and contained less delay, so these filters can be used in various applications such as pulse shaping FIR filter in WCDMA system, software design radio and signal processing system for high speed. In future the work to reduce the power consumption in large tap DA FIR filters could be performed.

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