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Implementation of UART with Status Register using Multi Bit Flip-Flop

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Abstract: *A UART (Universal Asynchronous Receiver and Transmitter) is a device allowing the reception and transmission of information, in a serial and asynchronous way. This project focuses on the implementation of UART with status register using multi bit flip-flop. During the reception of data, status register indicates parity error, framing error, overrun error and break error.In modern very large scale integrated circuits, Power reduction and area reduction has become a vital design goal for sophisticated design applications. Multi-bit flip-flop is an effective power saving implementation methodology by merging single bit flip-flops in the design. The underlying idea behind multi-bit flip-flop method is to eliminate total inverter number by sharing the inverters in the flip-flops. Based on the elimination feature of redundant inverters in merging single bit flip-flops into multi bit flip-flops, gives reduction of wired length and this result in reduction of power consumption and area.*

Keywords: *Clock buffer, Clock network, Multi bit flip-flop, status Register, Single bit flip-flop.*

I. Introduction

Universal Asynchronous Receiver Transmitter (UART) is a kind of serial communication protocol. UARTs are used for asynchronous serial data communication by converting data from parallel to serial at transmitter with some extra overhead bits using shift register and vice versa at receiver.

Optimizations in VLSI have been done on three factors: Area, Power and Timing (Speed). The implementation of multi-bit flip-flop is an effective method for clock power consumption reduction. By replacing Flip-Flops with multi-bit Flip-Flops power consumption can be reduced. By using single clock pulse the Multi-bit Flip-flop (MBFF) is designed so that the same functionality like two or more single-bit Flip-flop (SBFF) can be achieved. So in this project multi bit flip- flop is implemented in status register of UART. The timing performance of MBFF can be analyzed by simulating in Xilinx. As a result the Clock network such as clock buffer and gate delay can be reduced. So the total area used for designing is also reduced.

II. UART Concept

UART is a Universal Asynchronous Receiver-Transmitter, which is used to communicate between two devices. Most computers and microcontrollers include one or more serial data ports utilize to communicate with other serial I/O devices, such as keyboards and serial printers. Serial ports are also used to communicate between two computers using a UART in each computer and a crossover cable, which connects the transmitter of one UART to the receiver of the other, and vice versa. Serial communication uses a transmitter to send data, one bit at a time, over a single communication line to a receiver. You can use this method when data transfer rates are low or you must transfer data over long distances. Serial communication is popular because most computers have one or more serial ports, so no extra hardware is needed other than a cable to connect the instrument to the computer or two computers together.

A UART provides the means to send information using a minimum number of wires. The data is sent bit serially, without a clock signal. The main function of a UART is the conversion of parallel-to-serial when transmitting and serial to- parallel when receiving. The fact that a clock signal is not sent with the data complicates the design of a UART. The two systems (transmitter and receiver) contain separate and unsynchronized local clocks.The proposed design of UART, shown in Fig. 2, has LCR, Transmitter and Receiver as its functional units. All these blocks are explained in brief as course of rest of this section.

2.1 Line Control Register (LCR)

The line control register (LCR) is a byte register. It is used for precise specification of frame format and desired baud rate. The parity bits, stop bits, baud rate selection and word length can be changed by writing the appropriate bits in LCR.

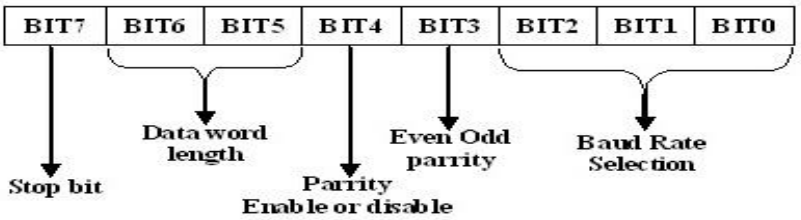

Figure 1: LCR format

2.2 UART Transmitter

The transmitter section accepts parallel data, makes the frame of the data and transmits the data in serial form on the Transmitter Output (TXOUT) terminal. Data is loaded from the inputs TXIN0-TXIN7 into the Transmitter FIFO by applying logic high on the WR (Write) input. If words less than 8 bits are used, only the least significant bits are transmitted. FIFO is 16-byte register. When FIFO contains some data, it will send the signal to Transmitter Hold Register (THR), which is an 8-bit register. At a same time, if THR is empty it will send the signal to FIFO, which indicates that THR is ready to receive data from FIFO. If Transmitter Shift Register (TSR) is empty it will send the signal to THR and it indicates that TSR is ready to receive data from THR. TSR is a 12-bit register in which framing process occurs. In frame start bit, stop bit and parity bit will be added. Now data is transmitted from TSR to TXOUT serially.

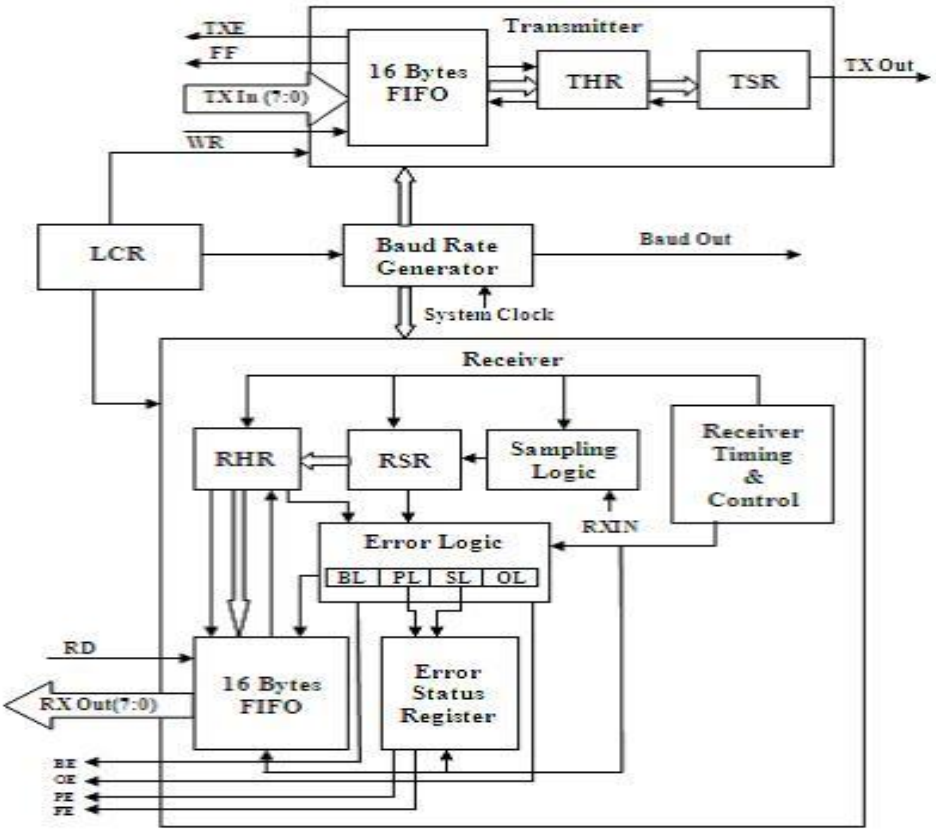

figure 2: UART Architecture

2.3 UART Receiver

The transmitted data from the TXOUT pin is available on the RXIN pin. The received data is applied to the sampling logic block. The receiver timing and control is used for synchronization of clock signal between transmitter and receiver. Initially the logic line is high whenever it goes low sampling and logic block will take 4 samples of that bit and if all four are same it indicates the start of a frame. After that remaining bits are sampled in the same way and all the bits are send to Receiver Shift Register (RSR) one by one where the entire frame is stored. RSR is a 12 bit shift register. Now if the Receiver Hold Register (RHR) is empty it sends signal to RSR so that only the data bits from RSR goes to RHR which is an 8 bit register. The remaining bits in the

RSR are used by the error logic block. Now if receiver FIFO is empty it send the signal to RHR so that the data bits goes to FIFO. When RD signal is asserted the data is available in parallel form on the RXOUT0-RXOUT7pins. The error logic block handles 4 types of errors: Parity error, Frame error, Overrun error, break error. If the received parity does not match with the parity generated from data bits PL bit will be set which indicates that parity error occurred. If receiver fails to detect correct stop bit or when 4 samples do not match frame error occurs and SL bit is set. If the receiver FIFO is full and other data arrives at the RHR overrun error occurs and OL bit is set. If the RXIN pin is held low for long time than the frame time then there is a break in received data and break error occurs and BL bit is set.

2.4 The UART Standard Data Format

Serial data are contained within frames of 8 data bits, as well as coded information bits. Between successive transmissions, the transmission line is held high. A transmission is initialized by a leading low start bit. Next to the leading low start bit comes 8 bits of data information, beginning with the LSB and afterwards represented at increasing significance order up to the MSB. Next to the 8 data bits comes the parity bit, representing the parity result of the 8 data bits. The parity bit can be encoded true based on even parity or odd parity mode. Next to the parity bit comes a trailing high stop bit indicating the end of a data frame.

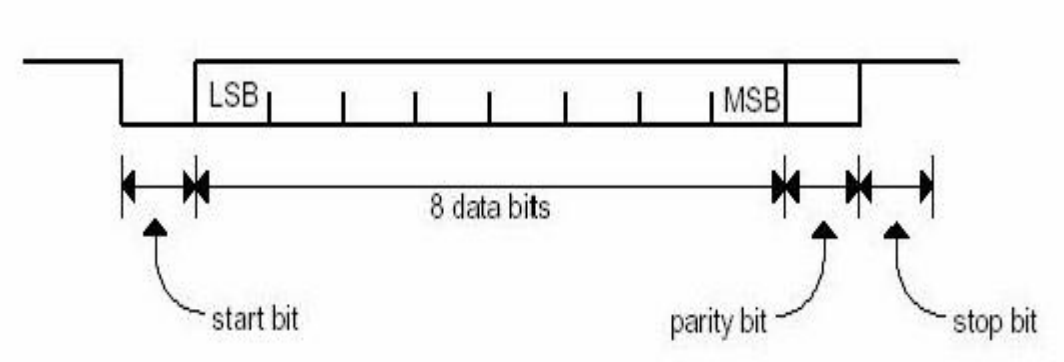

Figure 3: UART data format

III. Multi Bit Flip- Flop Concept

In this section, we will introduce multi-bit flip-flop concept. The proposed method for multi bit flip flop is merging of clock pulse. Before that, we will review single-bit flip-flop. Figure 3 shows an example of single-bit flip-flop. A single-bit flip-flop has two latches (Master latch and slave latch). The latches need "Clk" and "Clk' " signal to perform operations, such as Figure 1 shows.

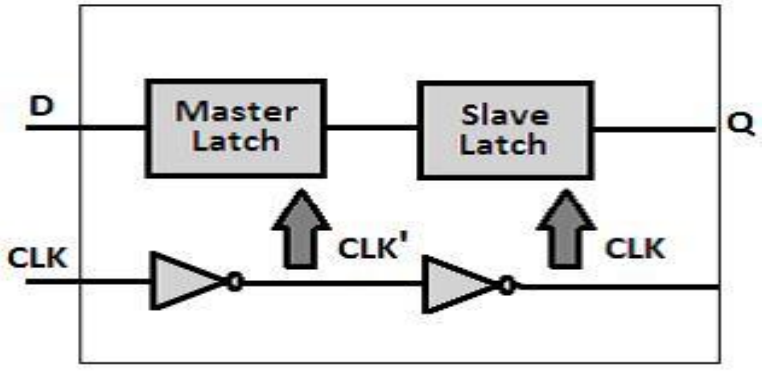

Figure 4: Single-Bit Flip-Flop

In order to have better delay from Clk-> Q, we will regenerate "Clk" from "Clk'". Hence we will have two inverters in the clock path. Figure 4 shows an example of merging two 1-bit flip-flops into one 2-bit flip-flop. Each 1-bit flip-flop contains two inverters, master-latch and slave-latch.

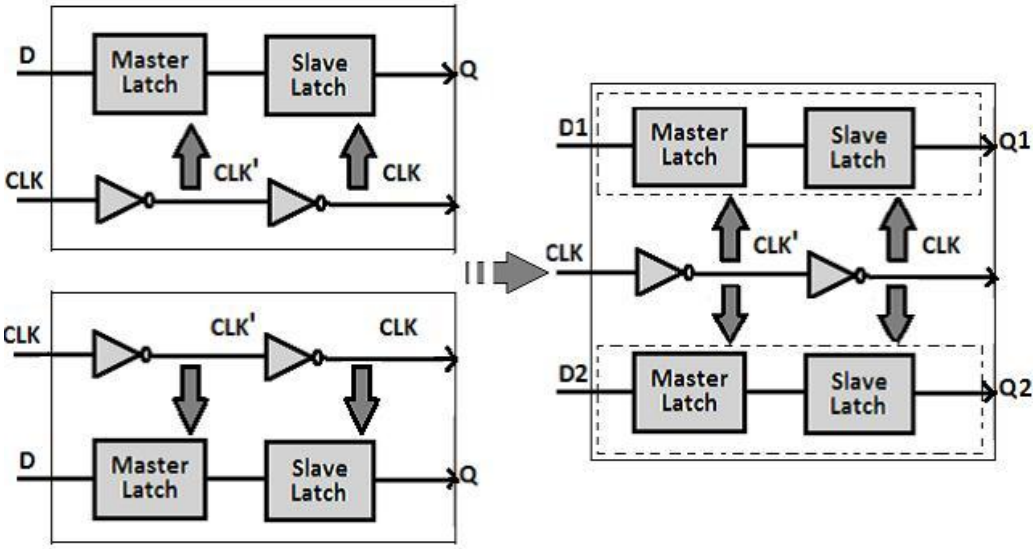

Figure 5: An example of merging two 1-bit flip-flops into one 2-bit flip-flop.

Due to the manufacturing rules, inverters in flip-flops tend to be oversized. As the process technology advances into smaller geometry nodes like 65nm and beyond, the minimum size of clock drivers can drive more than one flip-flop. Merging single-bit flip-flops into one multi-bit flip-flop can avoid duplicate inverters, and lower the total clock dynamic power consumption.

IV. Experimental Results

By implementing the multi bit flip-flop in UART with status register, it is simulated in Xilinx. The total power consumed by clock is 0.00263W. Atleast 20% of power is reduced when it is compared with normal UART with status register.In synthesis report, we can see only two clock buffers are used in UART with multi bit flip-flop. This indicates that the area is reduced. The simulation result for power and Synthesis report is shown in figure 6 and figure 7.

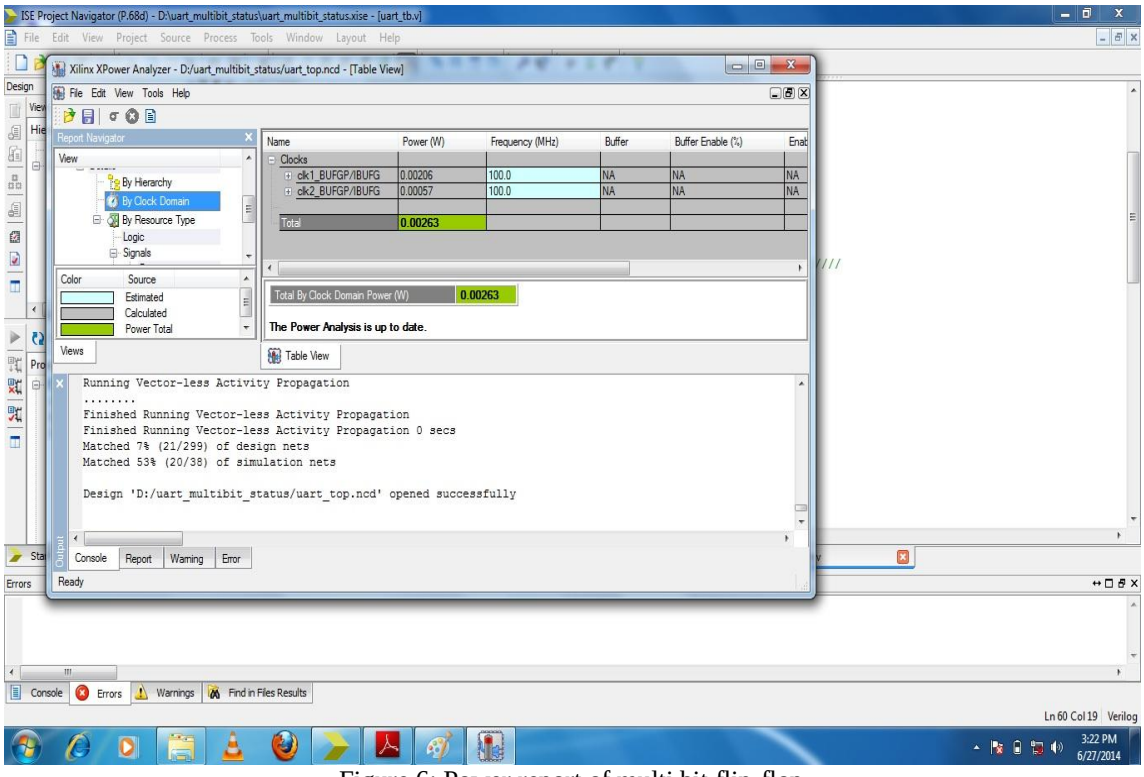

Figure 6: Power report of multi bit flip-flop

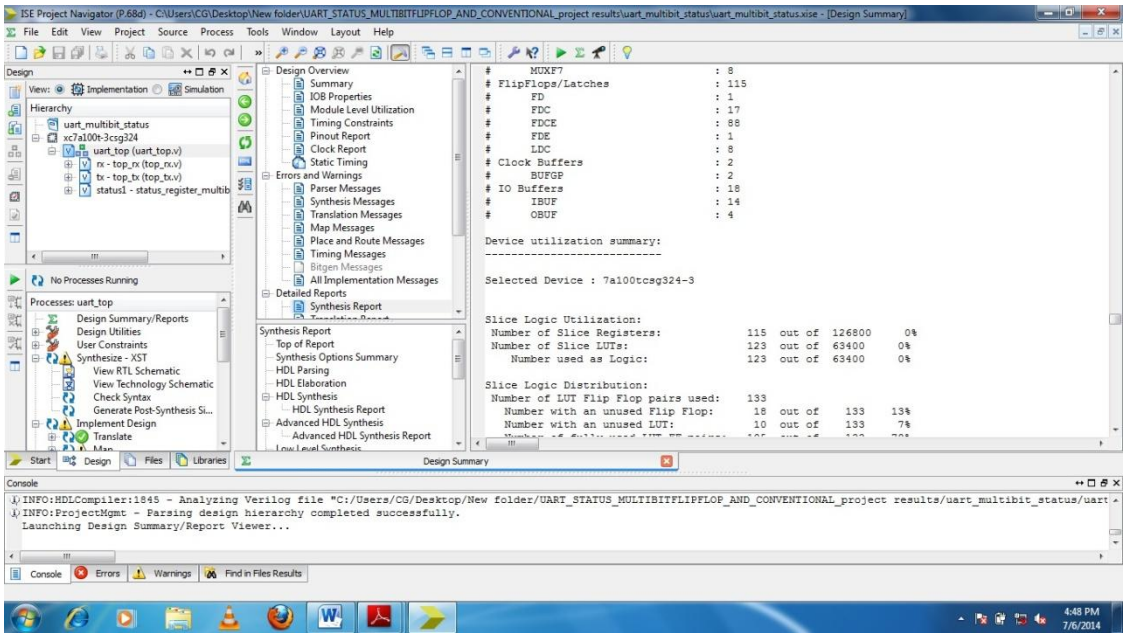

Figure 7: Synthesis report

V. Conclusion

In present VLSI design area is one of the important issues to be addressed. The proposed method is mplemented in Xilinx. Experimental results are targeted to number of flip flop usage and power used by clock buffer. Thus this proposed method is more suitable for reduction of hardware.

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