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An optimised multi value logic cell design with new architecture of many value logic gates

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Abstract: *Propose thesis work is a design of a Multi Logic Memory cell of four logic levels which can hold Logic 0, Logic 1, Logic 2 & Logic 3 and also propose an Interface module design between multi logic system with binary systems, thesis work can reduce the no. of wires required to parallel interface with normal memory and also can increase the speed of simple serial data transfer.*

I. Introduction

In year 2011 Mrs Fatma Sarica and Mrs. Avni Morgul publish in International conference on Electrical and Electronics Engineering and published in IEEE Journal they discuss in their abstract As Multi-valued logic circuits have been offered as a solution to general interconnection and chip area problem. In this paper they present a new latch and restoration circuit which improves the performance of the previously designed flip-flop circuit. The flip-flop is the usual building block of multilevel sequential circuits and may be used to design sequential circuits such as multilevel counter/dividers and other sequential circuits.
In year 2009, Mr. Ben Choi & Mr. Kunal Tipnis entitle 'New Components for Building Fuzzy Logic Circuits in Computer Science & Electrical Engineering' and 'Fuzzy Systems and Knowledge Discovery' paper were published in IEEE Explore. Journal they discuss in their abstract As This Paper Two New design of fuzzy logic circuit components. they designs of a new fuzzy memory cell and a new fuzzy logic gate . Different then a digital memory cell that can only store either a one or a zero, proposed multi logic memory cell store any value ranging from zero to one. Their cell can also be used as a D-type multi logic flip-flop, which is the first design of a D-type multi logic flip-flop.

II. Tools Used

Tanner EDA provides a complete line of software solutions that catalyze innovation for the design, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs). Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RF devices. Tanner EDA is a leading provider of easy-to-use, PC-based electronic design automation (EDA) software solutions for the design, layout and verification of analog/mixed signal ICs and MEMS.

III. Multi Level Digital Logic

Thesis Design is four level logic rather than two level logic (binary logic), physical interpretation is as shown in table 1

Table 1: The Physical Logic Levels of Proposed Multi value logic

Voltage range IN/Out	Multi level logic
0 to 1v	Logic '0'
1 to 3v	Logic '1'
3to 5v	Logic '2'
5 to 6v	Logic '3'

To make computation with four logic, in the thesis work design of four logic AND, four logic OR, four logic NOT & four logic Flip Flop have been done on EDA tool. Our Previous Research paper ref [10] already have description and implementation of this Circuits.

IV. Proposed Four Logic D-Flip Flop

Figure shown in below diagram is the design of Flip flop which are been proposed in the paper work. One thing is required to know that the logic GATE's are used in the circuits are also four value logic gates, working of this Gate are explained in Ref [10].

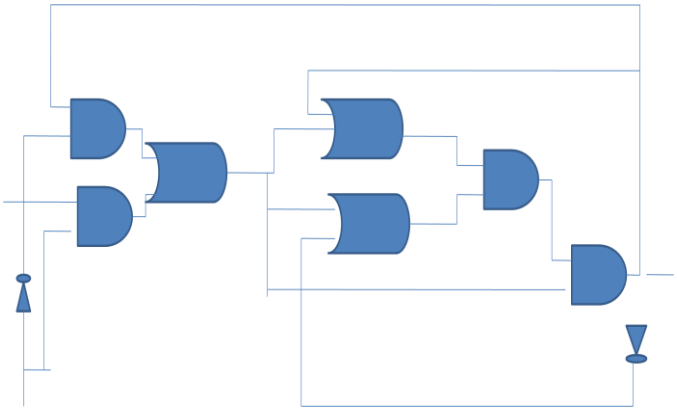

Fig 1: Four value Flip Flop Logical schematic

Four logic Flip flop		
Clock	Input	Output(stored value)
↑	0	0
↑	1	1
↑	2	2
↑	3	3

Table 2: Proposed Flip flop Truth table

As from the table above and from the table 1. The designing done on S-Edit with specified L= 44n and W=440n. NMOS and PMOS is been used and the T-Spice file been generated for the coding and parameter inserting the commands. The simulation time is chosen 600ns and W-edit is been used for generating the waveform. The S-edit schematic is been derived for proposed multi logic NOT, AND & OR logic gates.

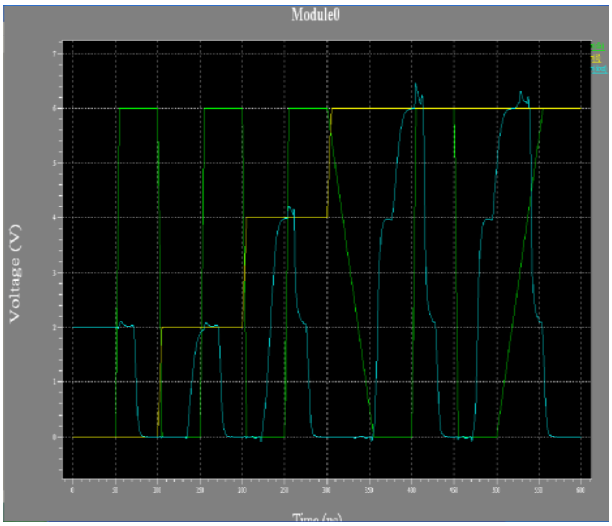

Fig 2 S-Edit Schematic of Proposed four logic F/F

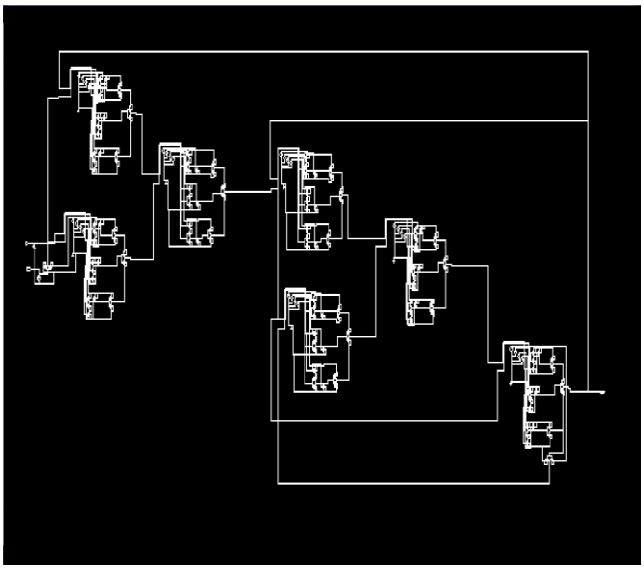

Fig 3 Simulation W-Edit results of four logic F/F

V. Binary To Four Logic Convertor

Figure below shows flow of the binary to multi logic conversion proposal. It is required because most of existing digital circuits support binary Boolean logic, and proposed design is four value logic. So this kind of convertor required for make proposed design compatible with existing circuits.

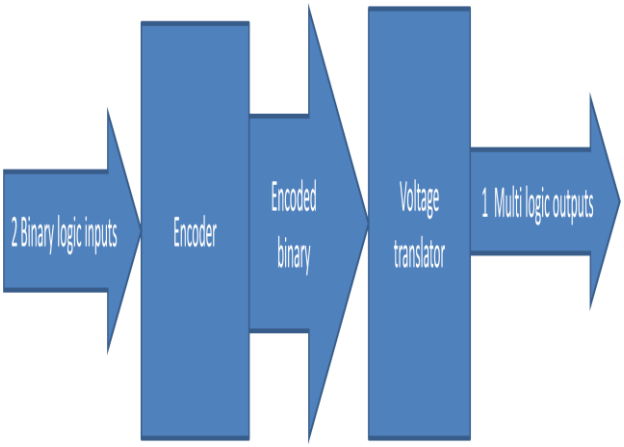

Figure 4 The Dataflow for binary to four logic conversion

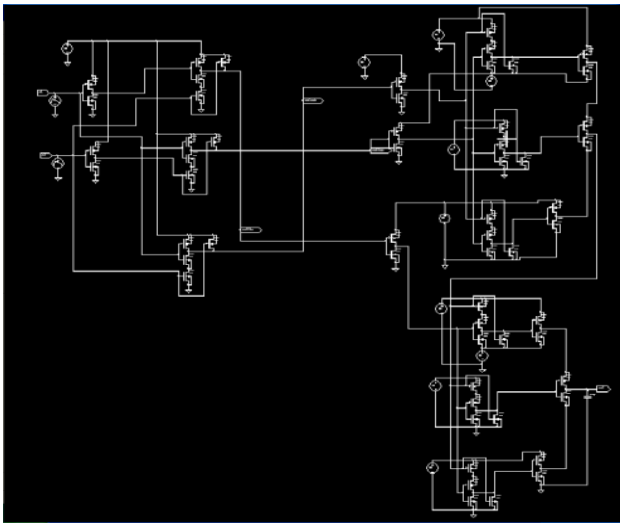

Figure 5: S-Edit Schematic of Convertor

Table shows the working of proposed convertor.

Table 3: Voltage level convertor for compatibility

Binary INPUT'S		Multi-logic output
0 (0-0.8 V)	0(0-0.8 V)	0 (0-1 V)
0(0-0.8 V)	1(3-5V)	1(1-3V)
1(3-5V)	0(0-0.8 V)	2(3-5V)
1(3-5V)	1(3-5V)	3(5-6V)

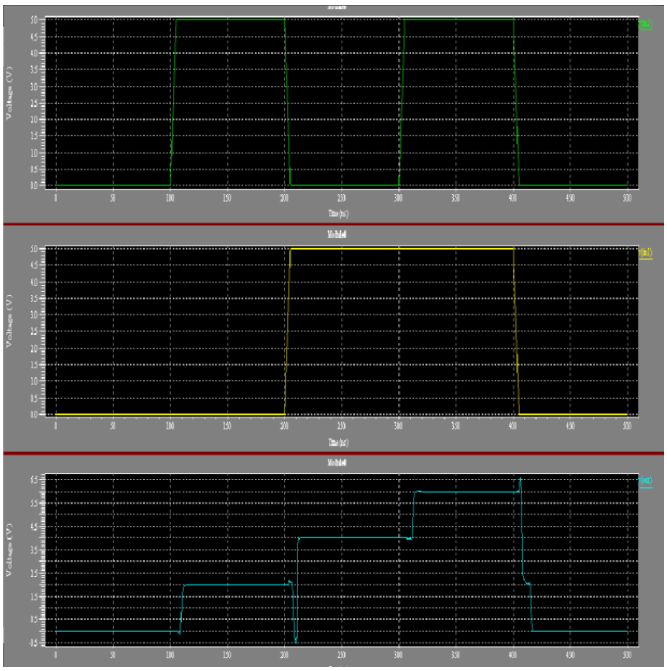

Fig 6 : WEdit Waveform for Proposed convertor

VI. Result

Table 4 Observed Result of each design

Design	MOSFET count	Average power consumed	
Designed four logic NOT	2	1.57 mw	27 ms
Designed four logic AND	18	2.34 mw	40 ms
Designed four logic OR	18	2.21 mw	39 ms
Designed four logic Flip Flop	130	3.95 mw	157 ms
Designed Binary to four logic convertor	58	3.91 mw	54 ms

Result's Analysis Table below shows the comparative analysis of proposed work with other existing design.

Table 5 Performance comparison with previous work

Multi logic Flip flop design			
	Base[1]	Base[2]	Thesis Designed work
No. of MOSFET	133	180	130
Average power consumed	4.15 mw	--	3.95mw

Problems Noise immunity is not significantly reduces as compare to binary logic.

VII. Conclusion

we can conclude that proposed work can be used for existing deign and by that way we can reduce power of data transmission by reducing number of data lines and reduce number of clock cycle by using four logic levels. We can half the number of flip flop using proposed flip flop. All can be achieved because of proposed binary to multi-logic convertor. Future scope of proposed work is that we can use proposed work with good noise margin and design can be further modify by reducing some more MOSFET.

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