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Power Quality Improvement Using FACT Devices

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Abstract: *Improvement of power quality has to be treated as a matter of at most importance in the open market economy due to the increased use of non linear loads. Several devices have been used to mitigate the power quality problems. Now a days researchers are concentrating on the use of FACT devices to overcome power quality issues. Unified Power Quality Conditioner is one among such FACT devices upon which this paper has concentrated for mitigating the Power Quality problems. Here a 3 phase 3 wire UPQC is realised using MATLAB/SIMULINK to mitigate voltage sag and swell as well as to maintain sinusoidal voltage and current at PCC irrespective of load dynamics.*

Keywords*: UPQC, Fact devices, Power Quality, Non-linear load, PCC.*

I. INTRODUCTION

The Power Quality is a factor of great concern in day today life. The increased use of electronic devices may cause pollution in the supply. The industrial loads are also very much sensitive to the voltage variations[1]. This may result in unsatisfactory performance of the system. Also there are necessities in medical field where the quality of supply matters. The variations in supply voltage may not be acceptable to a small extent, due to the high risk of rescuing a life. Another major area where the quality of supply matters is in research labs. For obtaining accurate output the quality of power has to be maintained at the supply side.

Several devices assure to mitigate power quality issues. Some of such devices includes passive filters, active filters and hybrid filters. But these devices have their own limitation[2]-[3]. Hence the use of CUSTOM power devices came prominent to mitigate power quality issues. Among them no devices can assure to mitigate more than two power quality problem at a time. Under such a circumstance, Unified Power Quality Conditioner (UPQC), which is a combination of DVR and STATCOM emerged by promising to maintain the quality of power at PCC, eliminates voltage distortions, current distortions, improvement of power factor and reduction in harmonics.

This paper includes the simulation of a three phase three wire UPQC. The simulation output reveals the effective performance of the system against voltage sag and swell. Also the system performance against the effect of load dynamics was satisfactorily evaluated.

II. SYSTEM OVERVIEW

The Unified Power Quality Conditioner (UPQC) is a multifunction conditioner. It comes under second generation of FACT devices. It mainly concentrates on improving the power quality at the utility grid. The UPQC consists of a series inverter and a shunt inverter which are linked by a dc link capacitor[4]-[6]. It also consists of series transformers and low pass filters. The role of LP filters is to attenuate the high frequency signals at the output of series converter that are generated by high frequency switching. The basic configuration of UPQC is given below in figure 1.

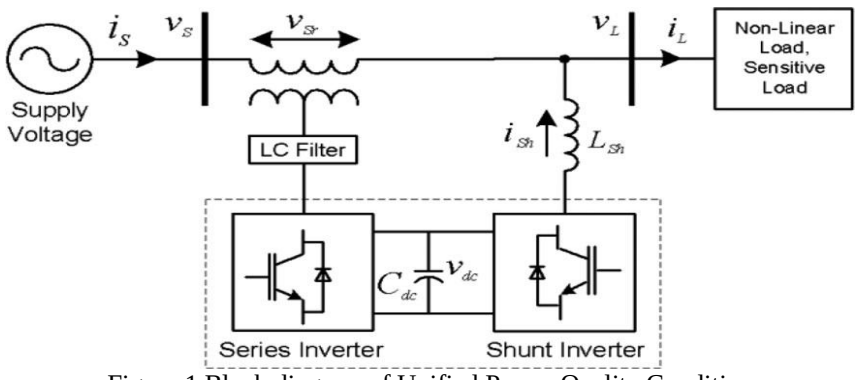

Figure:1 Block diagram of Unified Power Quality Conditioner

Where, i_s= Source current
v_s = Source voltage
v_{sr}= Voltage across series inverter
v_l = Load voltage
i_l = Load current
i_{sh} = Current injected by shunt inverter
C_{dc} = DC link capacitor
v_{dc} = DC link voltage.

Source: The AC loads or equipments on the power system is supplied by single or three phase source of power. Power quality related problems are similar for both these supply systems except an additional voltage unbalance compensation is needed in case of three phase systems. Here a three phase supply of 415V and frequency 50 Hz is used for carrying out the simulations.

Load : The use of non linear loads are increasing extensively now a day. They are responsible for introducing harmonics in the system which have their own adverse effects including power factor reduction. A 3 phase diode rectifier is used as the load in this paper to carry out the simulations. Also, later a linear load is being introduced into the system in order to validate the system performance against load dynamics.

Series inverter: Series inverter is connected in series with the supply and usually mitigates voltage distortions. It is also capable of handling supply voltage flickers and load voltage imbalance in the system. It is responsible for mitigating voltage sag in the system. The series inverter in generally is a DVR(Dynamic Voltage Restorer) which is connected in series with the system. The gating signals for triggering of series inverter are developed by comparing the reference signal with the load voltage. The reference signal is generated by comparing the voltages at the load and the source.

Shunt inverter: Shunt inverter is connected in shunt with the AC line. It usually deals with current distortions, improvement of power factor and reactive power compensation. It is also responsible for DC voltage regulation whereby we can achieve reduced DC capacitor rating. Inorder to provide electrical isolation of UPQC converters high pass filters are installed at the output of shunt inverter for quenching the current ripples.

In this paper, a three phase three wire UPQC is realised and the effect of load dynamics is studied. For this purpose a linear and a non-linear load is supposed to be injected to the system. Also the system response in mitigating the voltage sag as well as swell with a non linear load is also simulated.

III. Design Of Controllers

The major criteria in UPQC designing includes the designing of series inverter control, dc link voltage control and designing of shunt inverter control[7]-[8].

A. Control of Series Inverter

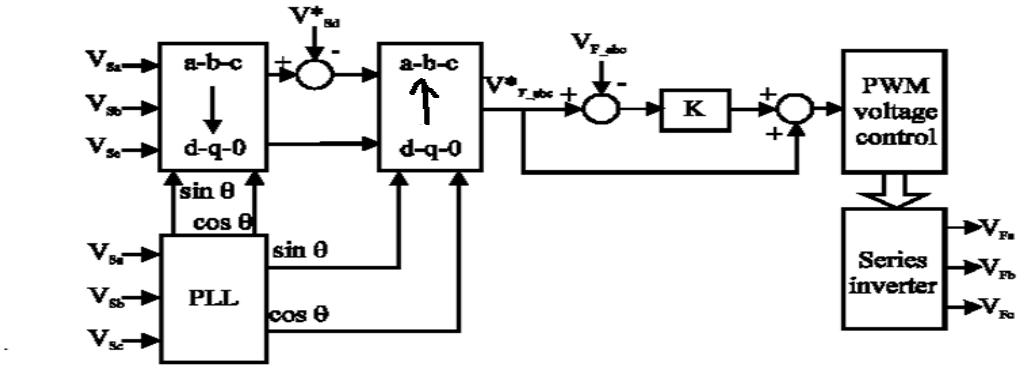

Figure 2. Series inverter control

The compensation of the entire voltage distortion is obtained by the proper controlling of the series inverter. The controlling of the series inverter also ensures a 3 phase balanced sinusoidal voltage.

The synchronous reference frame theory is applied in the controller by which the desired value of load phase voltage in d-q axis is compared with the load voltage for generating the reference signal. The response of the series inverter is optimized with the help of SPWM method. Figure 2 ,above shows the controller block of series inverter.

B. Control of Shunt Active Filter

Figure 3 shows the control diagram of the shunt inverter.The sine and cosine functions are extracted from the supply voltage using PLL. The measured load currents are transferred to dqo frame by the dqo conversion block. I_d is considered to be the active part and I_q is taken as the reactive part of the current. The role of PI controller is to track the difference which is taken as the error between the measured value and desired value of capacitance voltages. Thus generated reference current is converted back into abc frame with the help of dqo to abc transformation block. This is now compared with the shunt inverter output current and required pulses for switching the inverter gates are produced.

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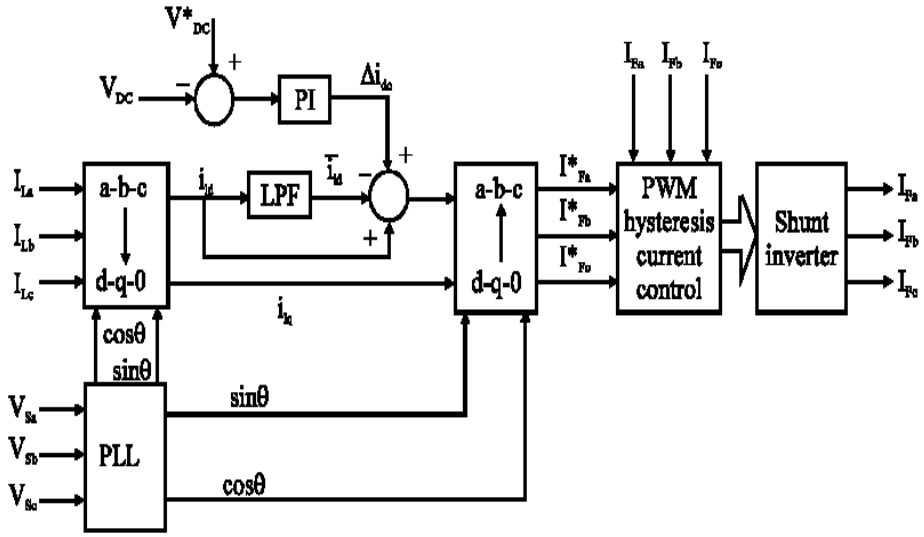

Figure 3. Control diagram of shunt inverter.

C. Control of DC link voltage

The DC link voltage is controlled by tracking the error that exists between the measured and desired value of the capacitance voltage. The control block of DC capacitance is given below in figure 4.

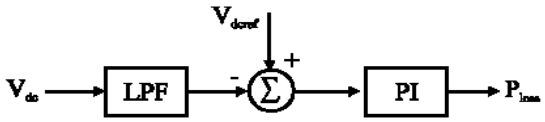

Figure 4. Single phase nine level inverter

It plays important role in control system DC voltage response is taken by the proper tuning of the PI controller. Increase in proportional gain leads to the instability of control system where as its reduction may cause decrease in the response speed of the control. In a similar way since the integral gain is responsible for correcting the steady state voltage error, its increase may results in correction of error at a faster rate. But it should be noted that too much of increase in integral gain ends in overshoot in the system response

IV. Simulation Results

Simulations have been performed in MATLAB/SIMULINK based on the Figure 1. The system parameters are chosen as given in table 1. Here the results are concentrated to the response of voltage and current waveforms at the point of common coupling. In the basic system simulink model due to the affect of nonlinear load applied the voltages and currents at PCC were found to be distorted. The system simulink model and their corresponding waveforms are given are given in figure 5 and figure 6 respectively[9]-[13].

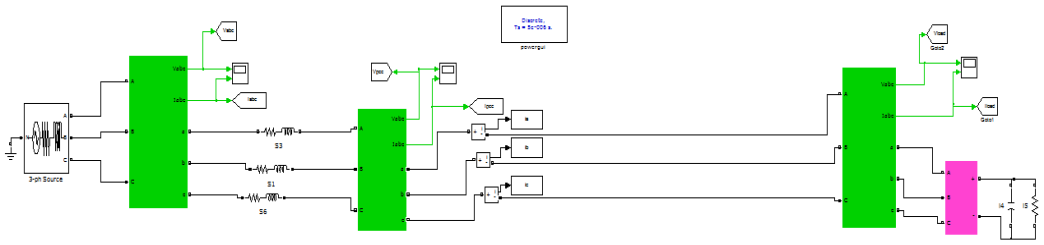

Figure 5. Simulink diagram of basic system

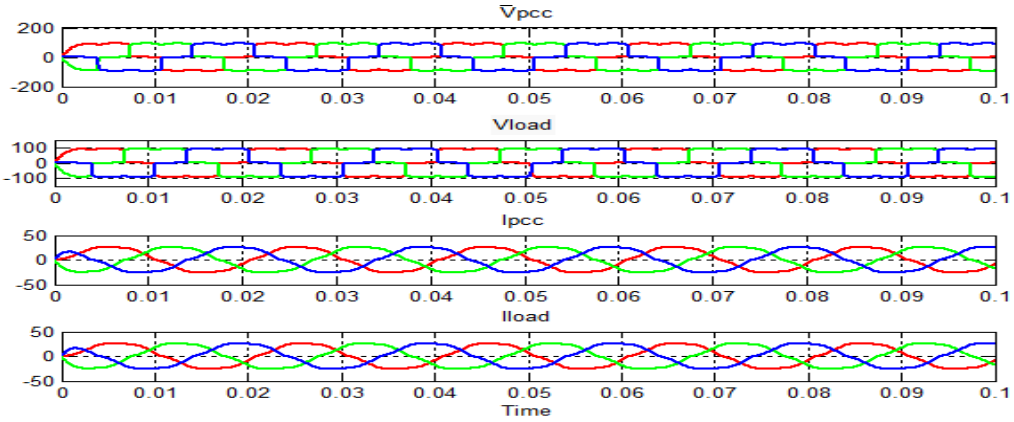

Figure 6. Wave forms of the basic system

The aim of UPQC is to maintain a sinusoidal volage and current at PCC inspite of any unbalance,or distortions at the load side. Hence a three phase three wire UPQC system was simulated inorder to justify its performance against voltage sag, swell and load distortions. Figure7 shows the simulink model of UPQC system.

A voltage sag of 50% the peak voltage system of the was introduced for the simulation time of 0.02 to 0.08s. The voltage and current waveforms at PCC and load side shows a reduction in value of current and voltage. Then the effect of UPQC in mitigating sag was tested by connecting it to the system. The waveforms shows that this system can effectively mitigate the voltage sag which occurred for a time duration from 0.02 to 0.08 s. The series inverter played its role in mitigating the sag. It injected the required amount of voltage for sag compensation. The waveforms of the uncompensated and compensated system are given in figure 8 and figure 9 respectively.

TABLE.1
SYSTEM PARAMETERS

System voltages	415V, 50 Hz
Non linear load	3 phase full bridge rectifier load of 1µF and 3.6Ω
Series interfacing transformer	1:1, 100V, 1000VA
Shunt VSI parameters	L_{sh}=2mH, C_{sh}=0.1µF
Series VSI parameters	L_s=13.5mH, C_s=0.004µF
PI controller gains	K_p=1, Ki=5

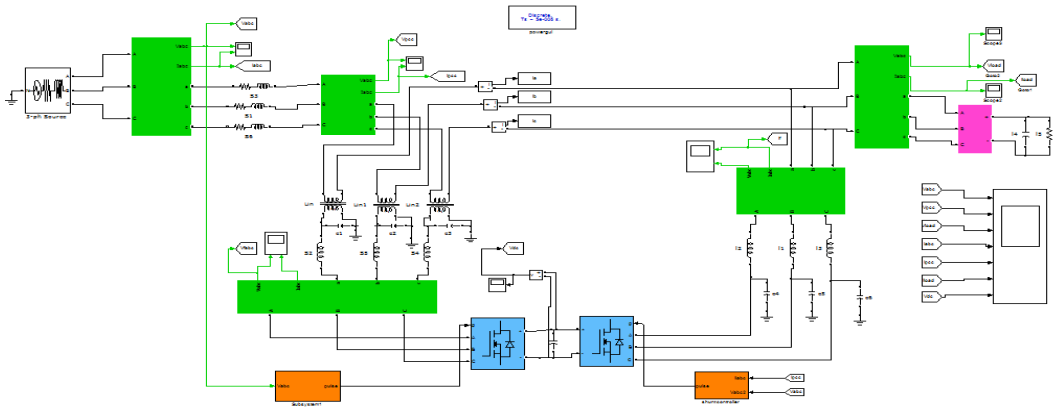

Figure 7. Simulink diagram of UPQC system

Next the system performance in mitigating voltage swell was analysed by introducing a swell in the system voltage from a period 0.2 to 0.6 using capacitor banks. The waveforms of voltages and currents at PCC and load end are as shown in figure 10. Here we can see a small increase in the value of voltages and currents due to the occurrence of swell. Now the system is connected with UPQC for validating its performance. It is seen that the UPQC eliminates voltage swell which occurred due to the capacitor bank switching. The waveforms of swell compensated system is given in figure 11.

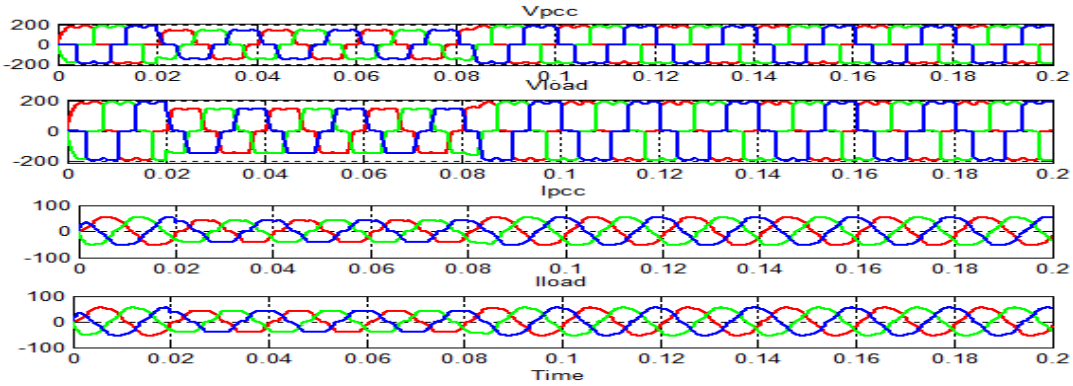

Figure 8. Wave forms of the uncompensated system during sag

The effect of load dynamics in the system with UPQC is studied by applying a three phase linear load together with the nonlinear load to the system. The effect of UPQC in the system shows that in spite of load variations it can maintain the voltage and current waveforms at PCC sinusoidal and to a desired value. This is shown in figure 12

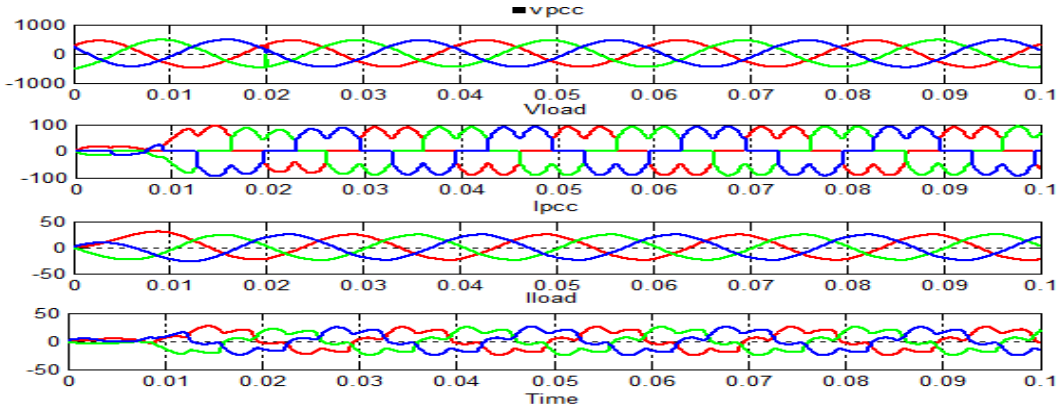

Figure 9. Wave forms of the sag compensated system

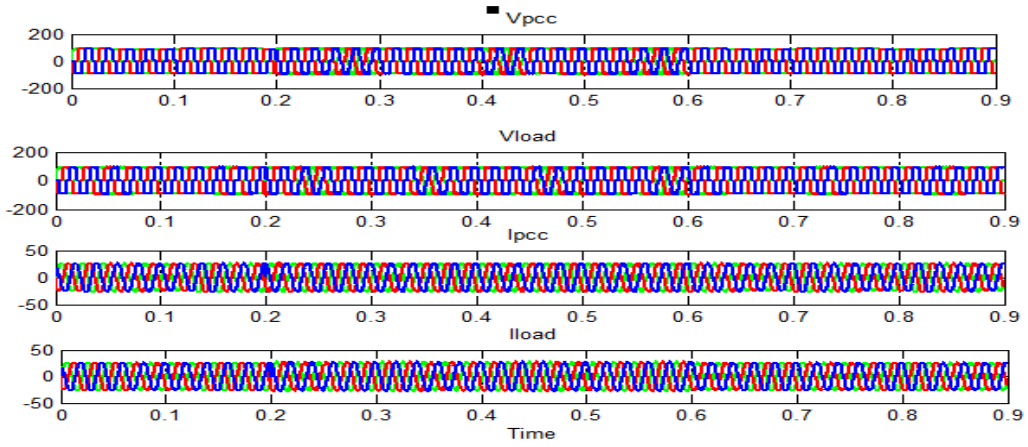

Figure 10. Wave forms of the uncompensated system during swell

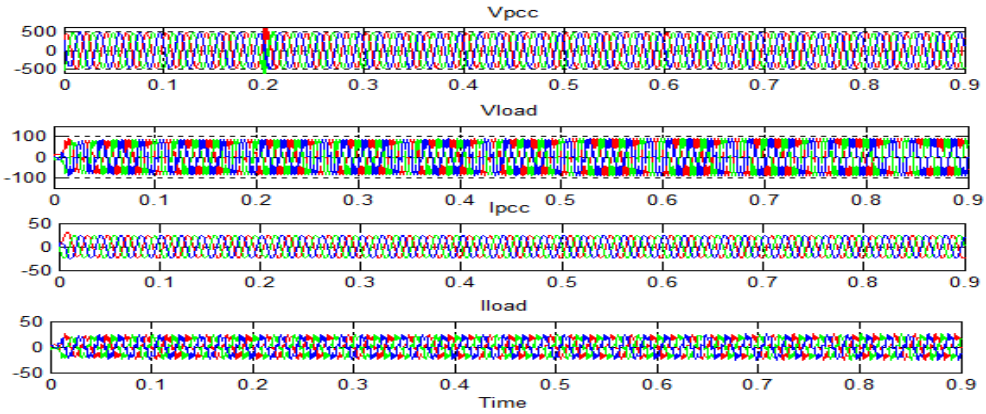

Figure 11. Wave forms of the swell compensated system

Also UPQC plays an important role in harmonic reduction. Table II compares the harmonics in a uncompensated and a compensated system during the occurrence of fault. This clearly reveals that the application of UPQC reduces the fifth and seventh order harmonics in the system.

TABLE.2

Before and after compensation

Harmonics	I_a (%)	I_a (%)	I_c (%)	I_a (%)	I_a (%)	I_c (%)
5^{th} order	7.65	5.46	8.23	3.60	0.78	4.11
7^{th} order	3.75	3.05	4.95	2.41	0.58	2.15

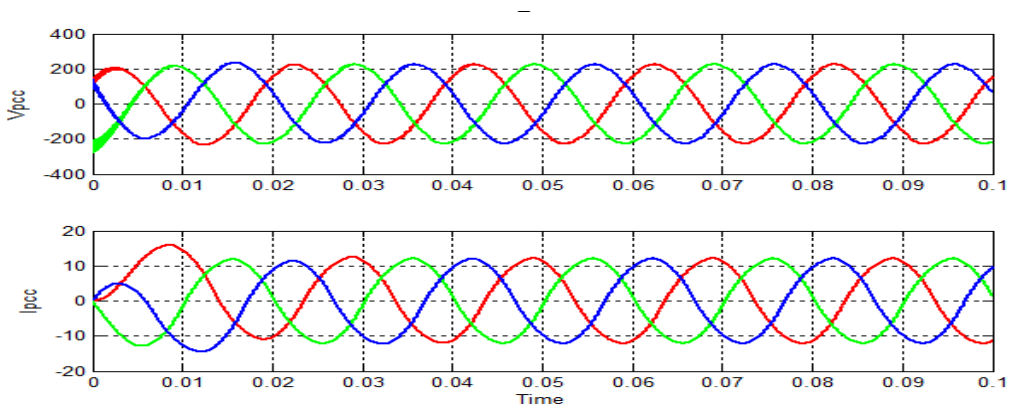

Figure 12. Waveforms at PCC showing the compensating nature of UPQC on applying load dynamics

V. Conclusion

The FACT devices are emerging as an important tool for reducing the power quality issues. Among them UPQC is seen to be more affective since it eliminates voltage distortions,current distortions, reduces harmonics, improves power factor etc. The simulation in this paper shows that UPQC ensures voltage stability, Harmonic reduction and desired accurate frequency.

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