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Reduction Of Leakage Current And Power In CMOS Circuits Using Stack Technique

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ABSTRACT: *Leakage Power is the major problem in CMOS VLSI circuits. There are various techniques to reduce this leakage power. Stack technique and Lector technique are two similar techniques to reduce the leakage power which have been discussed in this paper. In Stack technique instead of one PMOS or NMOS two PMOS or NMOS of half width are used respectively. And in Lector technique two leakage control transistors (one n-type and one p-type) are used between pull up and pull down network and gate of each leakage control transistor (LCT) is controlled by the source of other.*

***Keywords*:** *Leakage Control Transistor, Leakage Power, Lector Technique, Stack Technique*.

I. INTRODUCTION

In deep submicron engimes the major portion of total power consumption is leakage power. High power consumption reduces the life of battery in case of battery powered applications, So the motive of reducing the power is to actually increasing the service life of battery. We have one more option to reduce the leakage power is to reduce supply voltage as leakage power is the product of leakage current and supply voltage. But if we decrease the supply voltage and threshold voltage is constant than speed reduces because delay is inversely proportional to the difference of supply voltage and threshold voltage i.e. (V_{dd}-V_t) and if threshold voltage is also reduced than an exponential increase in sub threshold leakage current occur which will increase the leakage power five times so reducing the supply voltage is not fruitful.
In this paper stack technique is implemented on logic gates and full adder, full subtractor and decoder.

II. RELATED WORK

There are numerous methods proposed to control leakage power dissipation. In the paper entitled 'Design of Low Power CMOS Circuits using Leakage Control Transistor and Multi-Threshold CMOS Techniques' by U. Supriya, K. Ramana Rao,*Dept. of ECE, Pydah College of Engineering and Technology, Andhra Pradesh, India published in* Int.J.Computer Technology & Applications,Vol 3 (4), 1496-1500 two different techniques are proposed LECTOR and MTCMOS. Lector technique is already discussed above and in MTCMOS technique transistors of the gates are at low threshold voltage and the ground is connected to the gate through a high-threshold voltage NMOS gating transistor. The logical function of a gating transistor is similar to that of a sleep transistor. The existence of reverse conduction paths tend to reduce the noise margin or in the worst case may result in complete failure of the gate. Moreover, there is a performance penalty since high-threshold transistors appear in series with all the switching current paths. In this technique static power is reduced upto 20.99%.

Another paper 'Design of Leakage Power Reduced Static RAM using LECTOR' published by B. Dilip, P. Surya Prasad, *Dept. of ECE, MVGR College of* Engineering, *Andhra Pradesh, India in journal* (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 3 (3) implements the LECTOR in SRAM and says that this technique can reduce the leakage power upto 30-36%.

Another approach is given in paper 'COMPARISON AMONG DIFFERENT CMOS INVERTER WITH STACK KEEPER APPROACH IN VLSI DESIGN' published by Harshvardhan Upadhyay, Abhishek Choubey,kaushal Nigam in International Journal of Engineering Research and Applications (IJERA). We apply the stack keeper to generic logic circuits. Although the stack keeper incurs some delay and area overhead, the stack keeper technique achieves the lowest leakage power consumption among known state-saving leakage reduction techniques, thus, providing circuit designers with new choices to handle the leakage power problem.

III. METHODOLOGY

Stack technology and Lector technology both are based on stacking effect. According to this effect "a state with more than one OFF transistor between power supply and ground is far less leaky than the state with only one OFF transistor in the same path". In the stack technique instead of one transistor, two transistor of half width are used these transistors are connected in series. In the Lector technique two transistors (one PMOS and other NMOS) are introduced that are called Leakage Control Transistors (LCT's) in CMOS circuit. One LCT (PMOS) is connected to the pull up network and other LCT (NMOS) is connected to the pull down network. These both the transistors are connected in series and self controlled i.e. the gate of one transistor s controlled by the source of other so that one of the transistors is always near its cut off region.

GATE TYPE	*STATIC POWER (µW)*				*TOTAL POWER(µW)*	*DELAY (ns)*
	(0,0)	**(0,1)**	**(1,0)**	**(1,1)**		
NAND	0.185	0.252	0.185	1nw	2.094	0 .029
STACK NAND	0.248	0.278	0.173	0nw	1.333	0.101
NOR	0.358	0.165	0nw	0nw	2.017	0 .013
STACK NOR	0.342	0.166	0nw	0nw	1.195	0.044
AND	0.643	0.761	0.688	0.119	6.407	0.024
STACK AND	0.769	0.719	0.810	0.148	3.878	0.097
OR	1.416	0.283	0.130	0.130	6.839	0.025
STACK OR	1.706	0.398	0.202	0.202	5.755	0.158
	INPUT 0		*INPUT 1*			
INVERTOR	0.113		0nw		1.863	0.037
STACK INVERTOR	0.156		0nw		1.129	0.020

TABLE1. Static power, Total power and delay of all basic gates and their stack gates

IV. IMPLEMENTATION

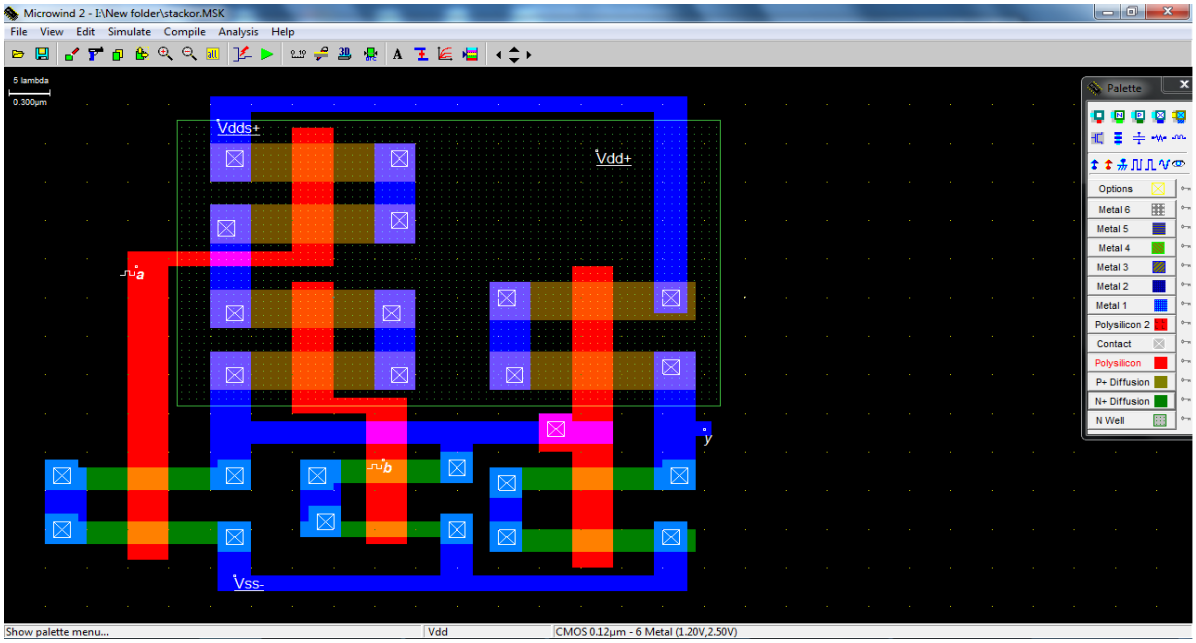

Fig.1: Two input Stack OR gate

This is the layout of 2 input Stack OR gate. In this circuit four PMOS transistors are connected in series and pair of two series connected transistors is connected in parallel. And the output of these transistors is given to the invertor to get final output of OR gate. Total six PMOS and six NMOS transistors are used. Input is given through input "a" and "b" and output is taken out through "y".

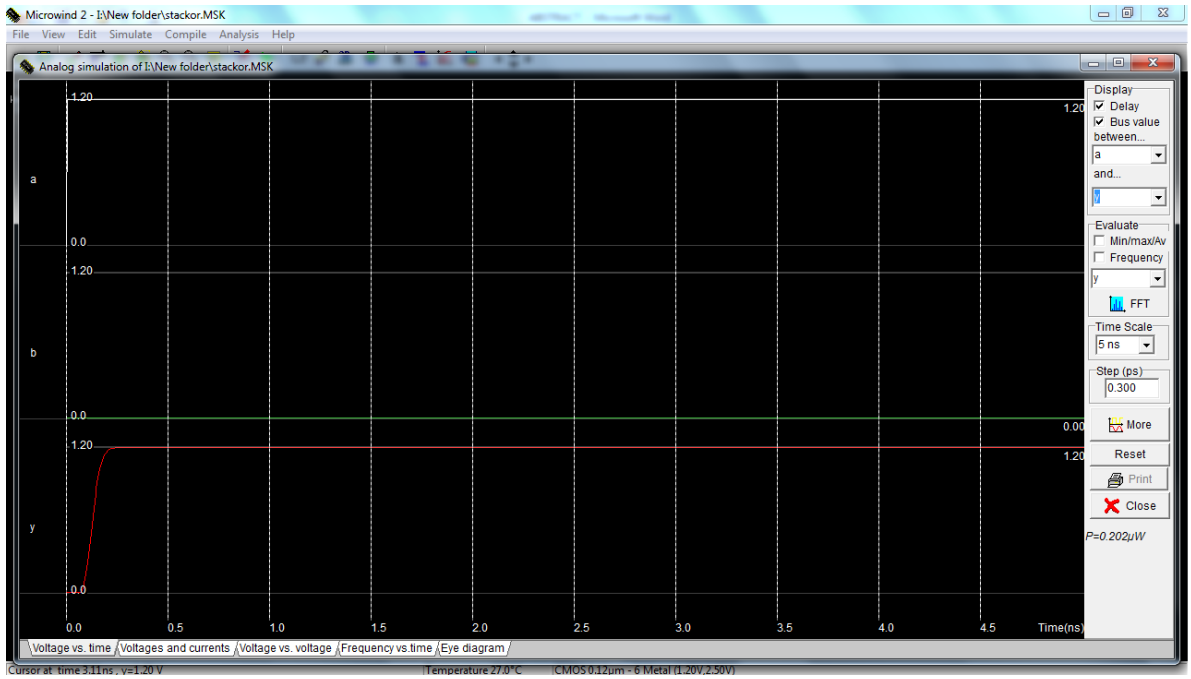

Fig.2: Timing Simulation of Stack OR gate

This is the analog simulation of the Stack OR gate. In this circuit output "y" is low when both the inputs "a" and "b" are low otherwise output is high. Total power is 5.755µw.In the above circuit input "a" is high and input "b" is low so the output value "y" is high. And total power is 0.202µw.

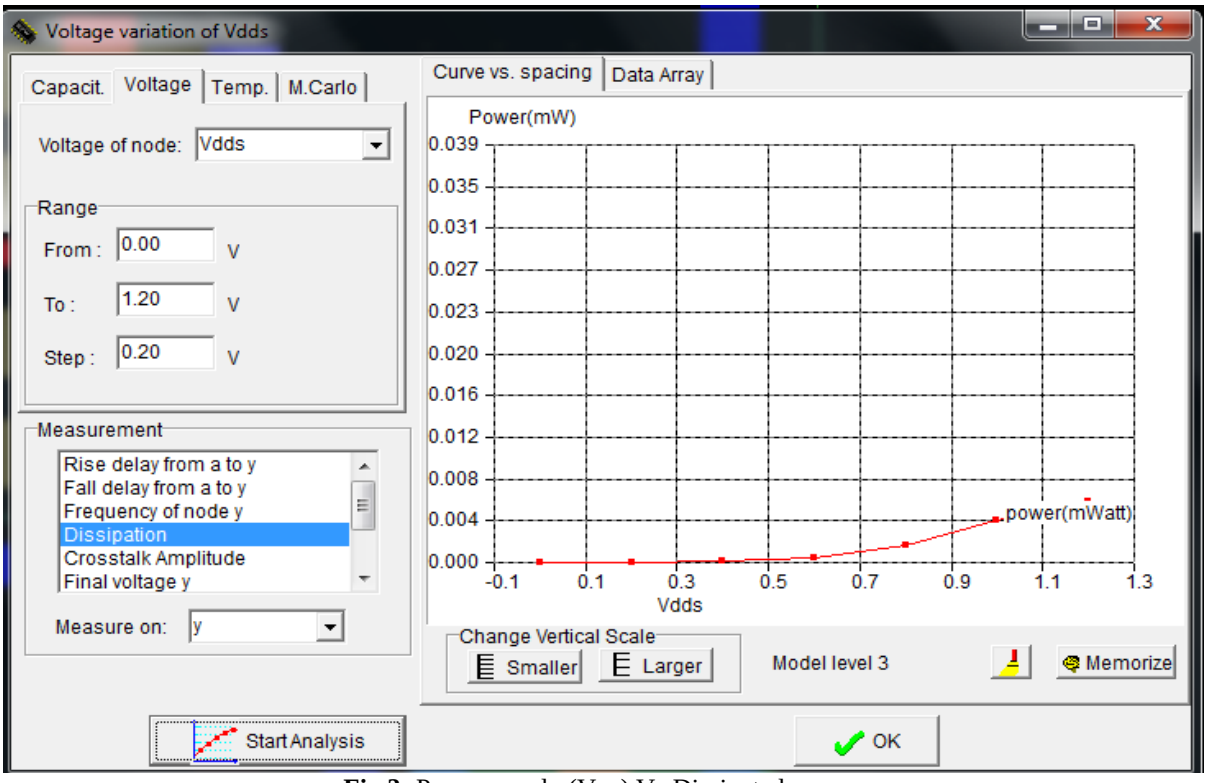

Fig.3: Power supply (V_{dds}) Vs Dissipated power

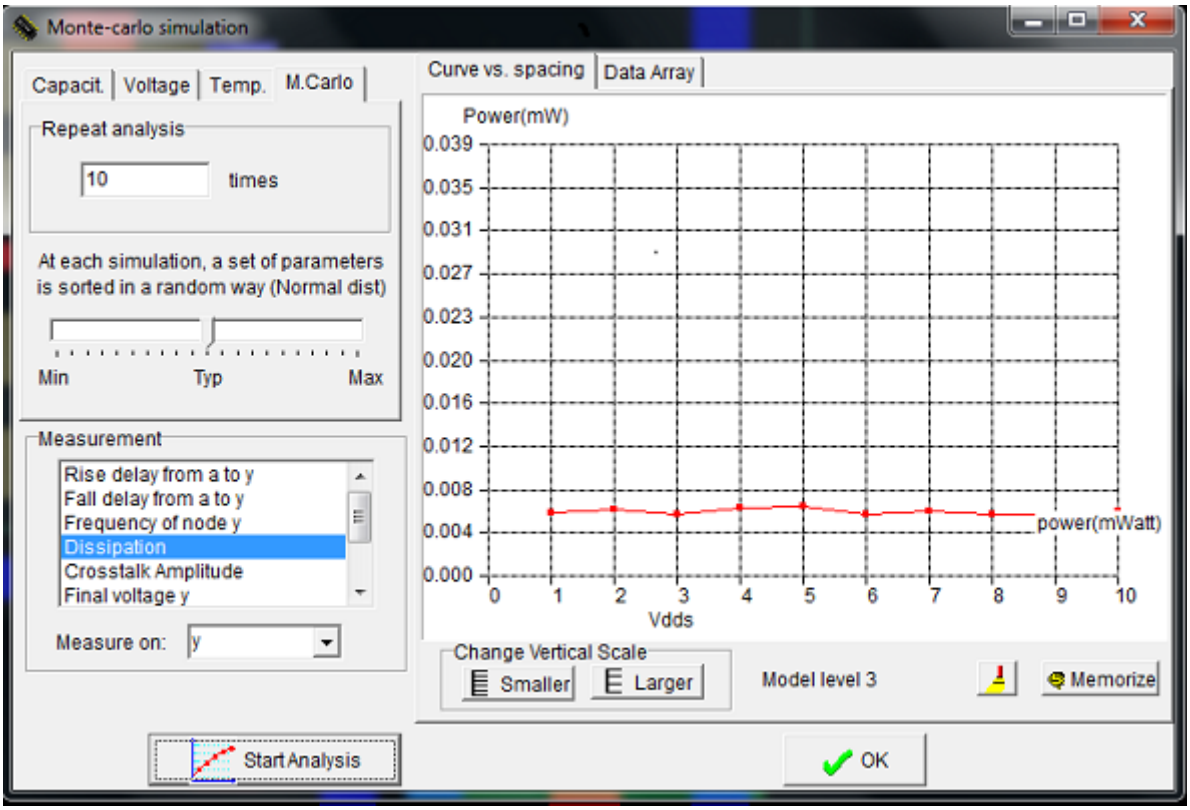

Fig. Monte Carlo simulation of power dissipation

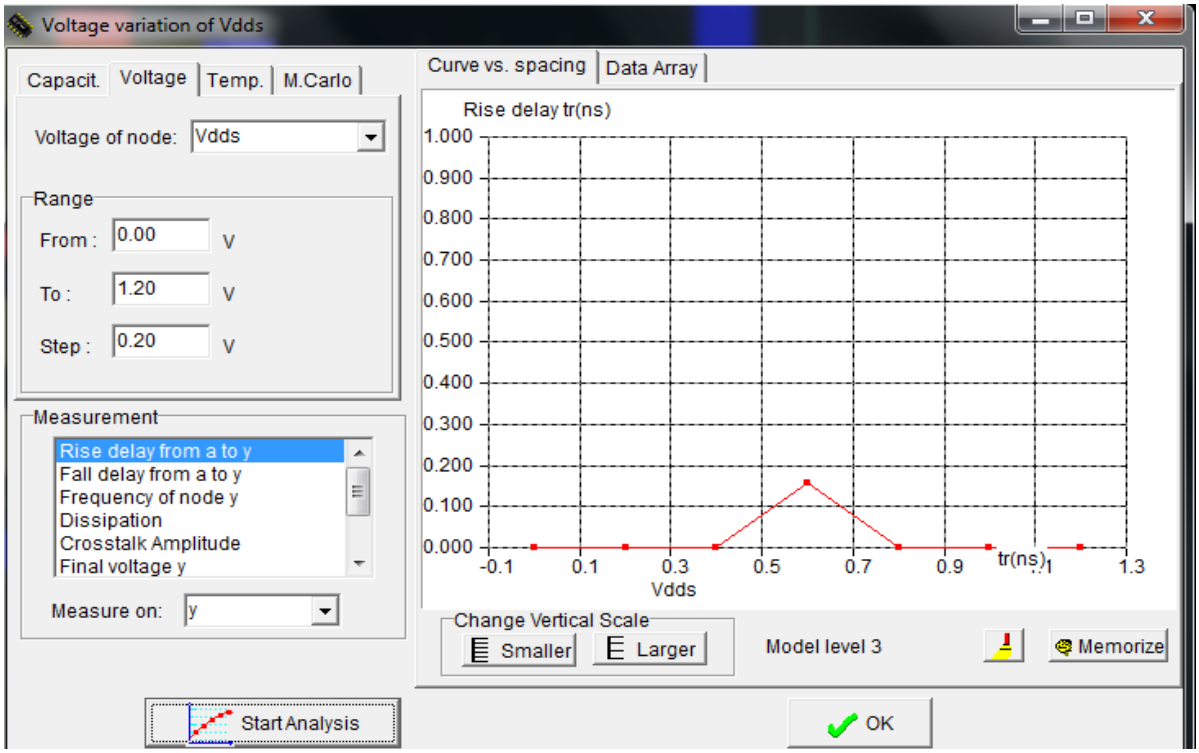

Fig.4: Power Supply (V_{dds}) Vs Rise delay

In the fig.3 and fig.4 graph "power supply Vs total power" and "power supply Vs Rise delay" is shown respectively. From node "a" to "y" the power is negligible i.e. 0.006mw. And from same node delay in the circuit is 0.156ns.

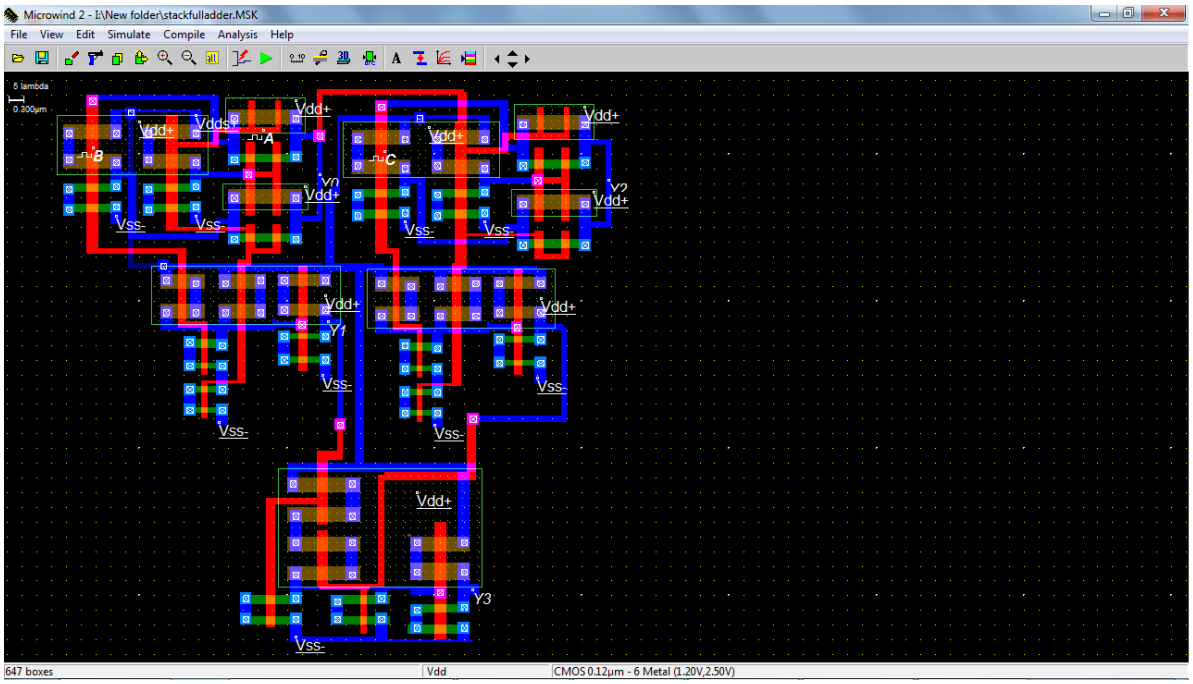

Fig.5: Stack Full Adder

In the fig5 Stack Full adder is shown where A, B, C are input nodes and Y_0,Y_1,Y_2 and Y_3 are output nodes. Output $Y_0$is the sum of input A and B, Output Y_1 is the carry of input A and B. Output Y_2 is the sum of all the inputs A, B and C. And Output Y_3 is the carry of three inputs A, B and C. Total Power of Full Adder in the above shown fig. is 25.525µw.

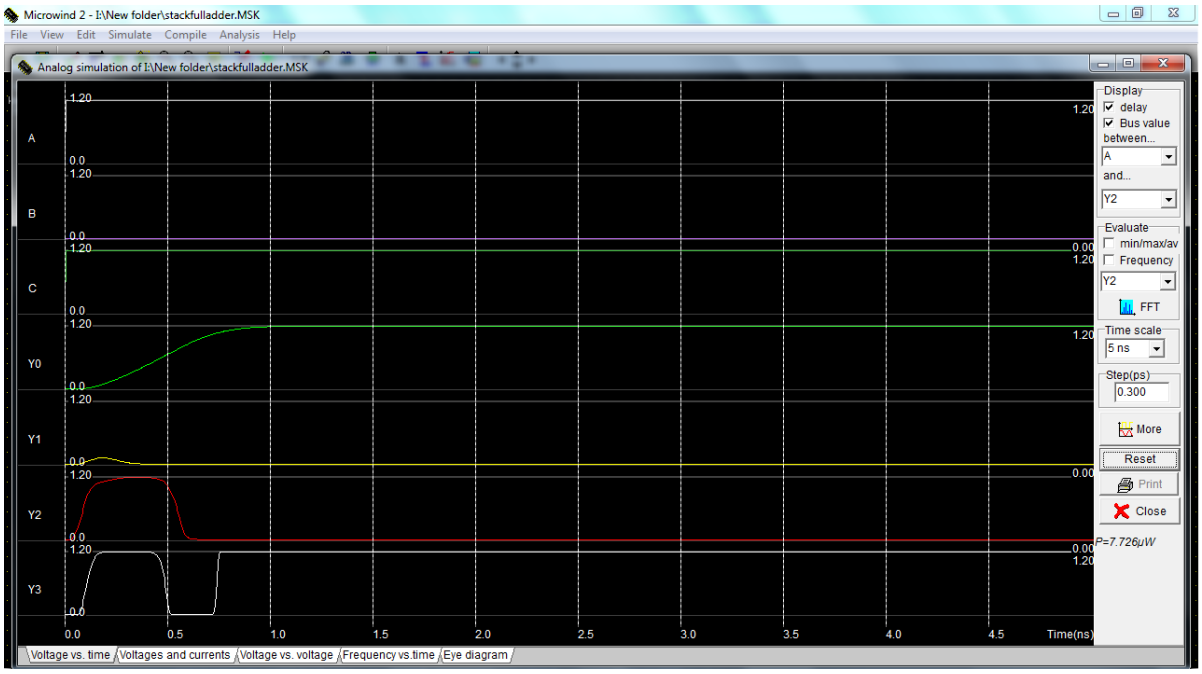

Fig.6: Timing Simulation of Full Adder

Fig.6 shows the timing simulation of Full Adder .In the given simulation inputs A and C are given '1' and input B is given '0' so the outputs are

Y_0= sum of input A and B = 1+0 = 1;

Y_1= carry of input A and B

= carry of the addition of 1 and 0

=0;

Y_2= sum of inputs A, B and C = 1+0+1
=0;
Y_3= carry of inputs A, B and C
= carry of the addition of 1, 0 and 1
=1;

So the outputs (Y_0, Y_1, Y_2, Y_3) are (1, 0, 0, 1) which is shown in Simulation also. The power in this case is 7.726µw.

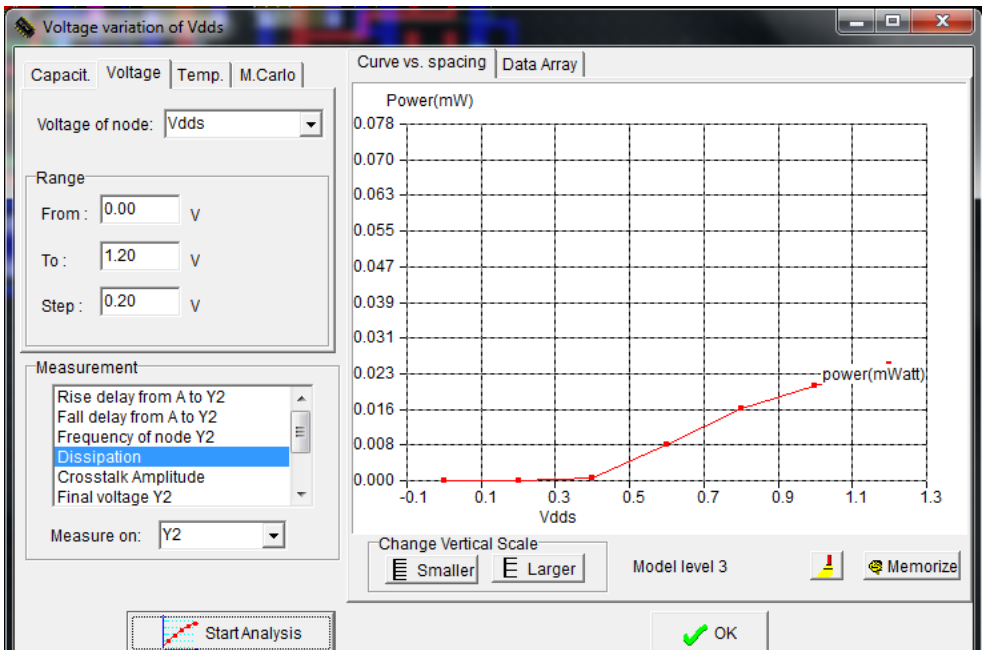

Fig.7: power supply Vs Dissipated power for Output Y_2

Fig.7 shows the graph between power supply and dissipated power for output Y_2. The dissipated power of the Full Adder for output Y_2 is shown 0.026mw which is similar for other outputs Y_0, Y_1, Y_3 there will not be any remarkable difference.

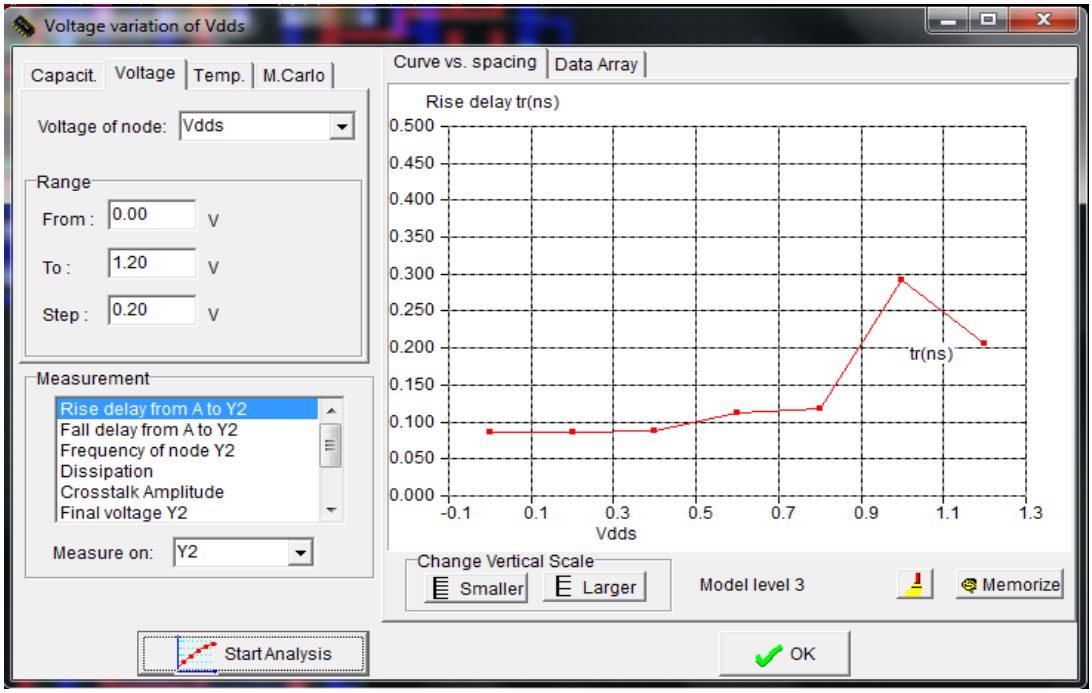

Fig.8: Power Supply Vs Propagation delay for Output Y_2

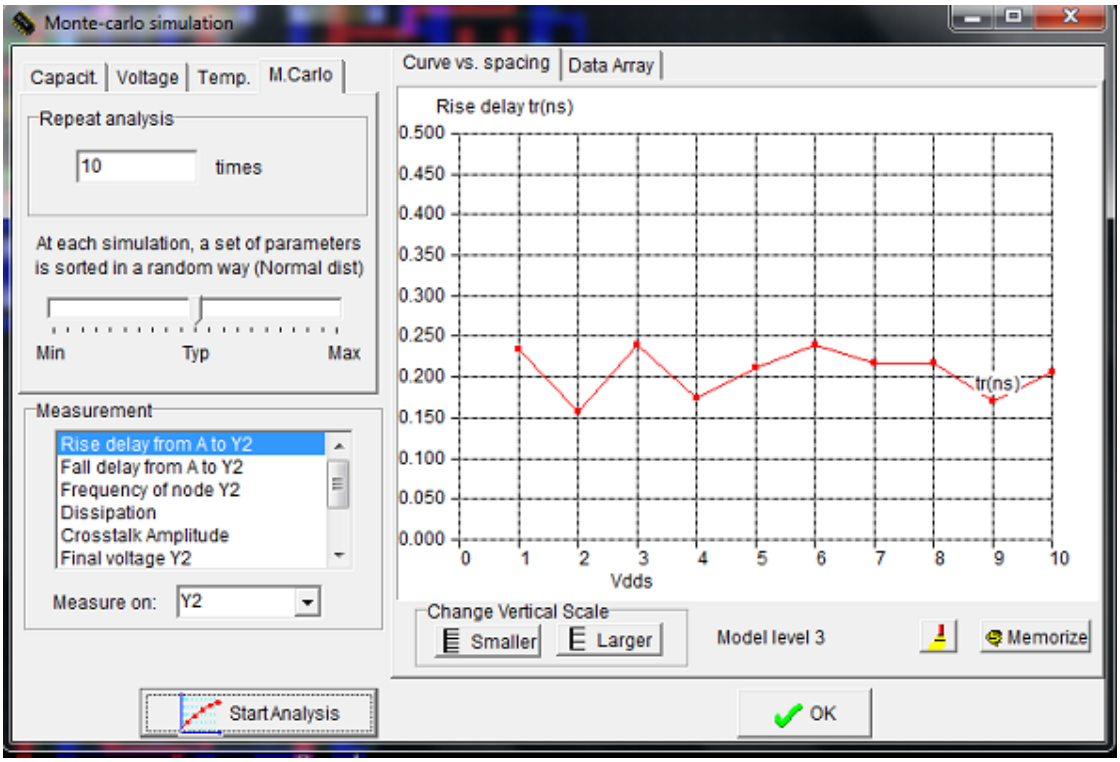

Fig. Monte Carlo delay simulation for output Y_2

Fig.8 shows the graph between Power supply and propagation delay for output Y_2.The propagation delay for output Y_2 is shown 0.292ns. Similarly the propagation delay for output Y_0, Y_1 and Y_3 are 0.372ns, 0.175ns and0.389ns respectively.

CIRCUIT TYPE	*POWER DISSIPATION(mw)*				*PROPAGATION DELAY (ns)*			
	Y_0	Y_1	Y_2	Y_3	Y_0	Y_1	Y_2	Y_3
HALF ADDER	0.013	0.013	--	--	0.029	0.091	--	--
FULL ADDER	0.026	0.026	0.026	0.026	0.372	0.175	0.292	0.389
HALF SUBTRACTOR	0.012	0.012	--	--	0.052	0.293	--	--
FULL SUBTRACTOR	0.026	0.026	0.026	0.026	0.156	0.287	0.174	0.254
DECODER	0.028	0.028	0.028	0.028	0.493	0.472	0.087	0.406

TABLE2. Power Dissipation and Propagation Delay of different circuits

In the Table1 the values of Static power, total power and delay of different logic gates and their respective stack logic gates are given .As it can be seen in the table that the total power of stack logic gates is lesser as compare to their respective logic gates. And this difference is not negligible even for small circuits.

In the Table2 Power dissipation and propagation delay of Half Adder, Full Adder, Half Subtractor, Full Subtractor and Decoder is calculated and given in table. In all these circuits stack technique is used. All these circuits have four output nodes and Power dissipation from a single node to different output nodes is almost constant for each circuit. Maximum worst case power dissipation for Half Adder is 0.013mw, for Full Adder is 0.026mw, for Half Subtractor 0.012mw, for Full Subtractor 0.026mw and for Decoder 0.028mw. Propagation delay from a single node to different output nodes is also calculated. Maximum delay from a specific node for Half Adder is 0.091ns to node Y_1 Similarly the maximum delay for Full Adder is 0.389ns to output node Y_3, for Half Subtractor is 0.293ns to node Y_1, for Full Subtractor is 0.287ns to node Y_1 and for Decoder is 0.493ns to node Y_0.

Stack technique has reduced the leakage power of the gates upto 40% it can be seen in the above tables. But at the cost of delay As it is shown while decreasing the leakage power upto some extent time delay has increased. But this increment in delay is tolerable because it is very less.

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