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Power Optimisation in the Design of Flip Flops Using Reversible Logic

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ABSTRACT: *Reversible logic design finds a major impact in the modern engineering world due to its low power consumption. More innovations in combinational as well as sequential circuits design reversible logic is going on,especially in shift registers and counters. An attempt is made for reversible logic to shift registers design using reversible D flip-flops has been proposed in this paper In the first phase with reversible logic with D flip-flop was deigned and analysed in terms of number of gates, garbage outputs with constant inputs. Serial in parallel out and serial in serial out with modified D flip flops are designed .In the second phase reversible T flip-flop for synchronous counter was attempted. In the third phase4 bit adder was designed and the results are compared with the conventional designs. The number of gated in D flip flops, and T flips are reduced by a factor of 2 and the garbage out put is improved by a factor of 4.In the shift register design both serial in serial out and serial in serial out ,the number of gates are reduced half of the conventional one and garbage out is increased by 2 fold.In the proposed 4-bit Reversible Synchronous Down-Counter number of gates are reduced by 4 times, and the power dissipation is reduced by a factor of 4.The simulations was carried out in Cadence tools.Vlsi laboratory .This paper conclude the reversible sequential circuits achieves better power and area trade off's .*

Keywords: *Reversible logic SIPO,SISO, Shift registers, quantum computing, reversible counters.*

I. INTRODUCTION

In the recent years the major criteria is how to reduce Power dissipation is one of the major goals in VLSI circuit design . R.Landauer proved, irreversible hardware computation results in energy dissipation due to the information loss, regardless of its realization technique [1]. Reversible logic circuits have theoretically zero internal power dissipation as there is no lose of information. Bennett showed that in reversible logic gates energy dissipation in a circuit is nil. The applications of reversible logic are quantum computation, optical computing, ultra low power CMOS design [3] and nano technology.

Even though some significant works ([4] - [10]) have been already done in the field of reversible sequential logic design, research on reversible counters are much attempted..

This paper proposes a novel concept on reversible sequential circuit design which includes shift registers and synchronous counters. Rest of the paper is organized as follows. Section 2 provides the idea of basic and necessary reversible logic gates used in this work. Section 3 provides the details about the proposed efficient reversible D flip-flop and its comparison with the existing work [5][6]. Section 4 provides the optimized reversible T Flip-flop and its comparison with the existing work [6]. Section 5 provides the proposed reversible shift registers such as serial-in serial-out and serial-in parallel-out and its comparison with the existing work [7]. Section 6 provides the proposed synchronous down counter using new reversible T flip-flop and its comparison with the existing work. Section 7 provides the Simulation results. Section 8 concludes the work.

1.1 Reversible logic Gates

Different reversible logic gates that are being used in the design are discussed here.

1.2 Feynman Gate

Fig. 1 shows a Feynman Gate. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

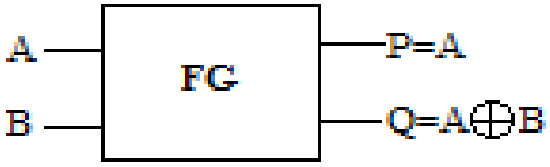


Figure. 1 Feynman Gate

1.3 Sayem Gate

Fig. 2 shows Sayem Gate [9]. A single Sayem Gate (SG) can be used to realize the function of D-Latch.

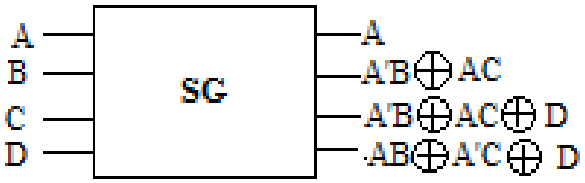


Figure. 2 Sayem Gate

1.4 Fredkin Gate

Fig. 3 shows the Fredkin Gate (FRG) [11]. This is the most widely used reversible gate.

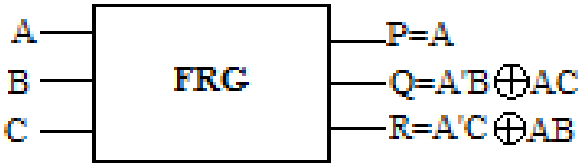


Figure. 3 Fredkin Gate

Peres Gate

Fig. 4 shows a Peres Gate (PG). It is also known as New Toffoli Gate (NTG). Functionally Peres Gate is equal with the transformation produced by a Toffoli Gate followed by Feynman Gate.

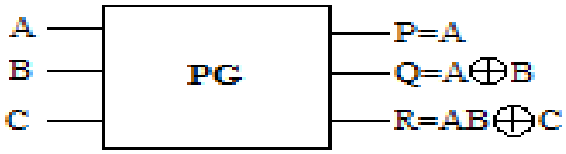


Figure. 4 Peres Gate

Proposed Reversible Positive Edge Triggered D Flip-flop

A flip-flop is a bi-stable electronic circuit that has two stable states and can be used as a one-bit memory device. The characteristic equation of D flip-flop is Q+ = D.CLK +Q (t-1).CLK'.

Figure5 shows the implementation of the Reversible Edge triggered D flip-flop using Sayem gate and the block diagram is shown in a Figure 6. The truth table for a Reversible edge trigged D flip-flop is shown in Table 1. And the comparison of the proposed design with the existing design has shown in Table 2.

Table I

Truth Table Of The Edge Triggered Reversible D Flip-Flop

CLK	D	Qt-1	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

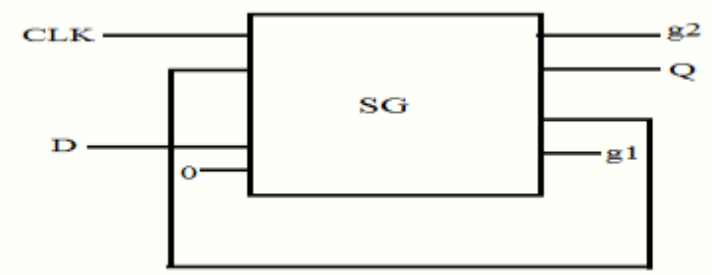


Figure. 5 Reversible edge triggered D flip-flop

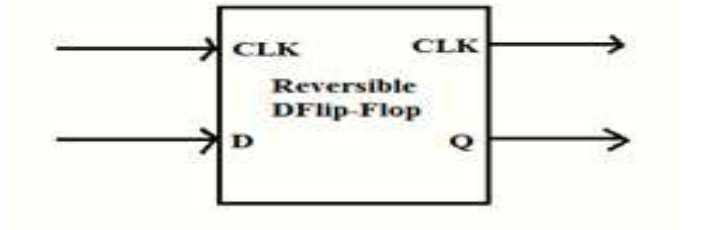


Figure 6 Block Diagram of Reversible D flip-flop

II. TABLE

Comparison Of Proposed Reversible D Flip-Flop With Existing Design

	No. of Gates	Garbage Outputs	Constant Inputs
Proposed design	**1**	**2**	**1**
Existing Design	**2**	**2**	**1**
Improvement Factor	**2**	**--**	**--**

Proposed Reversible Positive Edge Triggered T Flip-Flop

In this section we propose the construction of a Master-Slave T Flip-flop using reversible gates. The truth table of the T Flip-flop is given in Table 3. The reversible design is shown in Figure 7 and the corresponding block diagram is shown in Figure 8. The reversible realization of T Flip-flop has two SG gates and one Feynman Gate. And it has two constant inputs and it produces three garbage outputs. The comparison of the proposed design with the existing designs is given in Table 4.

Table III

Truth Table Of The Positive Edge Triggered Reversible T Flip-Flop

CLK	T	Q_{t-1}	Q
0	0	0	0
1	0	0	0
0	0	1	1
1	0	1	1
0	1	0	0
1	1	0	1
0	1	1	1
1	1	1	0

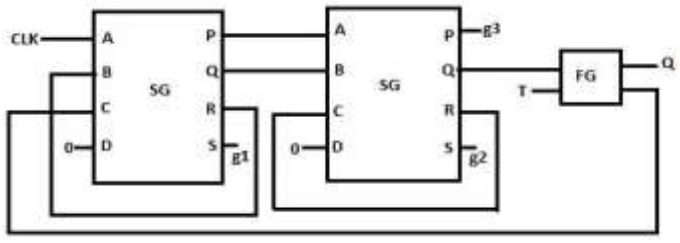


Figure. 7 Reversible Positive Edge Triggered T Flip-flop

Figure . 8 Block Diagram of Reversible T flip-flop

Table
Comparison Of Different Reversible T Flip-Flop With Existing Design

	No. of Gates	Garbage Outputs	Constant Outputs
Existing[9]	**10**	**12**	**10**
Existing[14]	**5**	**3**	**2**
Proposed Design	**3**	**3**	**2**
Improvement Factor	**3.3**	**4**	**5**
Improvement Factor	**1.6**	--	--

III. DESIGN OF PROPOSED REVERSIBLE SHIFT REGISTER

The shift register is one of the most extensively used functional devices in digital systems. A shift register consists of a group of flip-flops connected together so that information bits can be shifted one position to either right or left depending on the design of the device. This section proposes several types of shift registers including SISO, SIPO shift registers [7].

3.1Proposed 4-bit Reversible SISO Shift Register

SISO shift register is the simplest shift register that contains only flip-flops. In right shift register, output of a given flip-flop is connected to the data input of the next flip-flop at its right. Each clock pulse shifts the contents of the register one bit position to the right.

The serial input is provided to the left most flip-flop and the serial output is the output of the right most one. Figure 9 shows the proposed 4-bit reversible SISO shift register built from 4 reversible clocked D flip-flops.

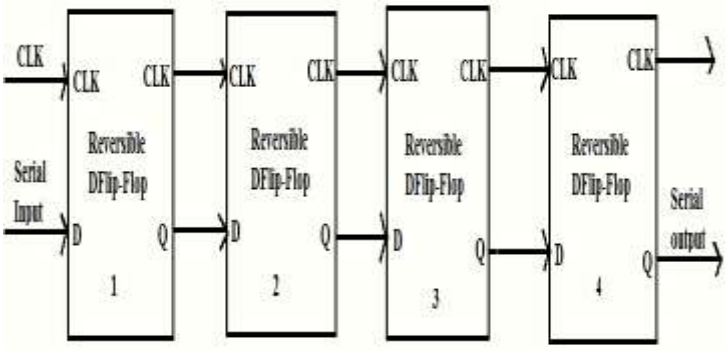


Figure. 9 Proposed Reversible 4-bit SISO Shift Register

Table V
Comparison Of Proposed Reversible 4-bit SISO Shift Register With Existing Design

	No of Gates	Garbage Outputs	Constants Inputs
Proposed Design	**4**	**5**	**4**
Existing Design[4]	**8**	**5**	**4**
Improvement Factor	**2**	--	--

3.2 Proposed 4-bit Reversible SIPO Shift Register

A SIPO shift register is similar to SISO shift register. It is different in that makes all the stored bits available as parallel outputs. Reversible implementations of SIPO shift register using clocked D flip-flops is shown in Fig.10.

The serial data are entered to the SI input reversible left most flip-flop while the outputs O1, O2, O3, O4, are available in parallel form the Q output of the flip-flops.

The comparison of the proposed design with the existing is shown in Table 6.

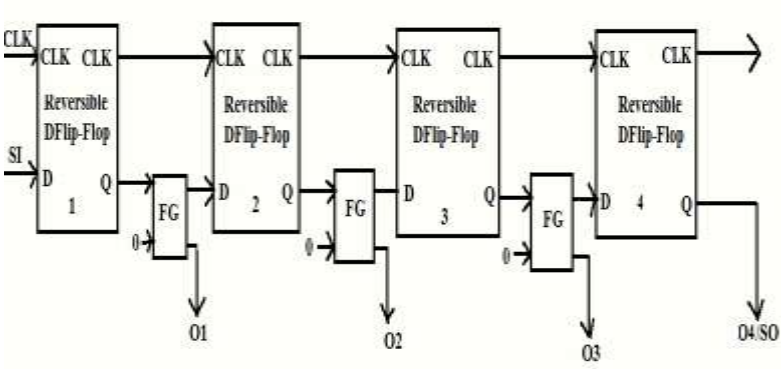


Figure. 10 Proposed 4-bit Reversible SIPO Shift Register

Table VI
Comparison Of Proposed 4-Bit Reversible Sipo Shift Register With Existing Design

	No of Gates	Garbage Outputs	Constants Inputs
Proposed Design	**7**	**5**	**7**
Existing Design[4]	**11**	**5**	**7**
Improvement Factor	**1.57**	--	--

IV. DESIGN OF REVERSIBLE SYNCHRONOUS COUNTERS

In the synchronous counters, the count pulses are applied directly to the control/CLK inputs of all the Flip-flops. Synchronous counters have regular pattern and can be constructed using flip-flops and gates.

Proposed 4-bit Reversible Synchronous Down-Counter

The reversible design of the above 4-bit Synchronous down Counter is shown in Fig. 11. The proposed RSJ gates are used to produce the copy of the Q output of the T Flip-flops. The Peres gate is used to realize the AND function. The proposed reversible synchronous counter design contains 15 reversible gates, 13 constant inputs and produces 12 garbage outputs.

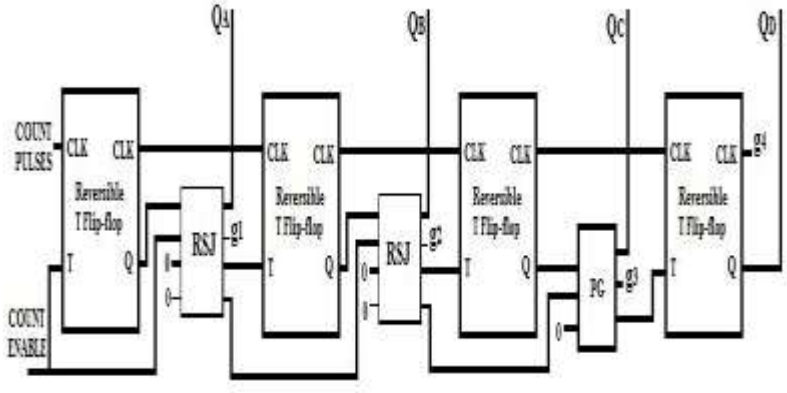
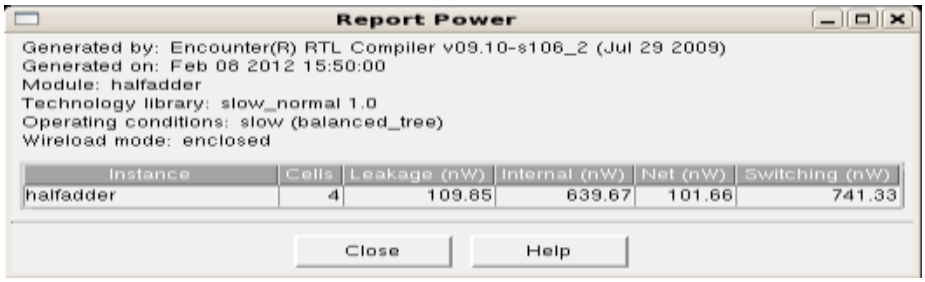
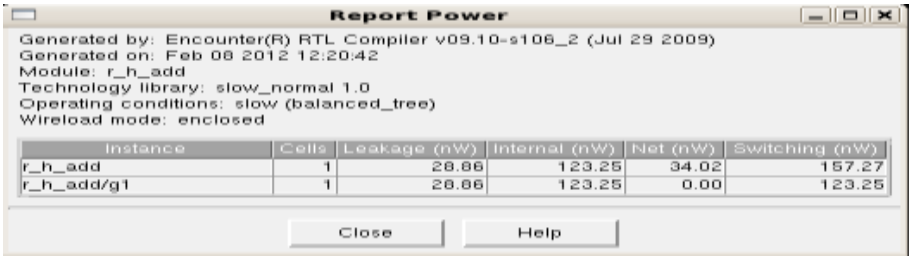


Figure. 11 Proposed 4-bit reversible synchronous down counter

Simulation Results in Cadenc Synthesis Tool Conventional Half DDER



A. Reversible Half Adder



V. CONCLUSIONS

The reversible 4-bit shift registers using reversible edge triggered D flip-flop such as SISO, SIPO was designed . The reversible 4-bit synchronous down counter using Proposed T flip-flop are designed , proposed designs are compared with the existing design and are tabulated.

From the table the number og gated in D flip flops, and T flips are reduced by a factor of and the garbage out put is improved by a factor of 4.In the shift register design both serial in serial out and serial in serial out ,the number of gateds are reduced half of the conventional one and garbage out is increased 2 times.In the Proposed 4-bit Reversible Synchronous Down-Counter number of gates are reuced by 4 times, and the power desipation in the half hadded circuit is reduced by a factor of 4. The proposed reversible sequential circuits achieves better power and area trade off's compare to the conventional sequential circuits which is shown in the results. The proposed reversible sequential circuits design ALU , reversible processor etc. This work forms an important move in building large and complex reversible sequential circuits for quantum computers. The future work could be to develop efficient reversible timing circuits and reversible controller circuits.

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