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Design of Approximate Multiplier Architecture Using Static Segment Method for Audio Signals

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ABSTRACT: *Now a day's, the energy constrained devices in DSP is grown .These applications use fixed point arithmetic operation to perform matrix multiplication & while exhibiting ability, it is essential to improve the valuable energy of multiplication. In this paper, an approximate multiplier architecture is designed by using static segment method. This architecture can meet the demand of less delay and area efficiency for an audio signal. Here different multipliers are used in approximate multiplier architecture to check which performs well .Those multipliers are Radix-4 Booth Multiplier, Vedic Multiplier.*
The delay and area of Radix-4 Booth Multiplier is more efficient than that of Vedic Multiplier.

Key words : Digital Signal Processing, Multiplication, Valuable Energy

I. INTRODUCTION

Battery capacity and power budget are limited for embedded and mobile computing devices .So achieving high energy efficiency is a key design objective for them. In digital signal processing and classification applications these devices use some keys which are required frequently. To further improve energy efficiency of executing such applications, first specialized processors are often integrated in computing devices .At same voltage and technology generation ,specialized processors can improve energy efficiency more compared to general purpose processors. Firstly ,we design and train these algorithm with floating-point numbers, because of power and area costs, it is converted into fixed point. By doing this conversion it leads to computational accuracy loss, which does not affect the quality and accuracy of DSP classification applications. Multipliers that can be used in DSP applications for convolution, filtering, matrix multiplication and it is a energy hungry component .In microprocessors and DSP algorithms mostly performs addition and multiplication about 70%, so for this operation it influences the implementation time.

Second, various DSP and classification applications mostly depends on complicated probabilistic mathematical forms and are framed to process data that normally consists of noise. Thus, for some counting error, they display delicate degeneration in overall DSP quality and classification accuracy on behalf of destructive failure .Such counting error tolerance has been exploited by trading accuracy with energy consumption .Using floating points arithmetic ,initially these algorithms are designed and trained, and then it converts into fixed point arithmetic because the power and area costs for supporting floating points in embedded counting .

In spite of this transformation process ,it leads to some loss of counting precision, it does not particularly affect the feature of DSP and the precision of classification applications due to counting error steadiness .Most of such algorithms thoroughly perform matrix multiplication as their fundamental operation, while a multiplier is typically an inherently energy-hungry component**.**

III APPROXIMATE MULTIPLIER ARCHITECTURE METHODS

Two methods are used in approximate multiplier architecture to improve the valuable energy .

- **Dynamic Segment Method(DSM) :**
  we are taking 'm' bit continuous segment from an 'n 'bit operands , i.e leading one bit operand of 'n' bit operand.

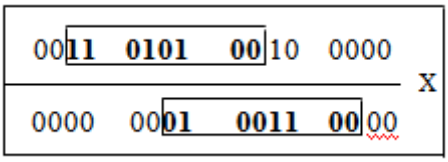

Fig 1: Example for selecting '8' bit segment from '16' bit operand

With two 8 bit segments and two 16 bit operands , we can perform multiplication using 8x8 multiplier. By using this above example , for a 16x16 multiplication even with 8x8 multiplier we can achieve an accuracy of 99.4%.
DSM requirements

(a) Two LOD'S
(b) Two n-bit shifters to place the leading one bit position of each and every n-bit operand to the MSB then the m-bit segment is applied to m x m multiplier.
(c) A 2n-bit shifter is used to expand a 2m-bit result to 2n-bits
To satisfy these requirements, m should be greater than or equal n/2.

In this Dynamic Segment Method ,the LOD's cost is very high & the area used for the development of architecture is also increases inorder to overcome this drawback static segment method is came into existence.

- **Static Segment Method (SSM) :**

SSM simplify the circuit and selects m-bit segments and then steers to the m x m multiplier by
(a) By replacing n-bit LOD'S with (n-m) input-OR gates.
(b) Replacing two n-bit shifters with m-bit 2-to-1 multiplexers and
(c) To replace 2n-bit shifter with 2n-bit 3-to-1 multiplexer.

The segment for each operand is taken from one of two possible segments in an n-bit operand, a 2m-bit result can be expanded to a 2n-bit result by left shifting the 2m-bit result by one of three possible shift amounts.
(a) When both the segments are from lower m-bit segment then no shift
(b) When both the segments are from upper m-bits segments then 2x(n-m) shifts
(c) When the two segments both are from upper ones and lower one's then (n-m) shifts.

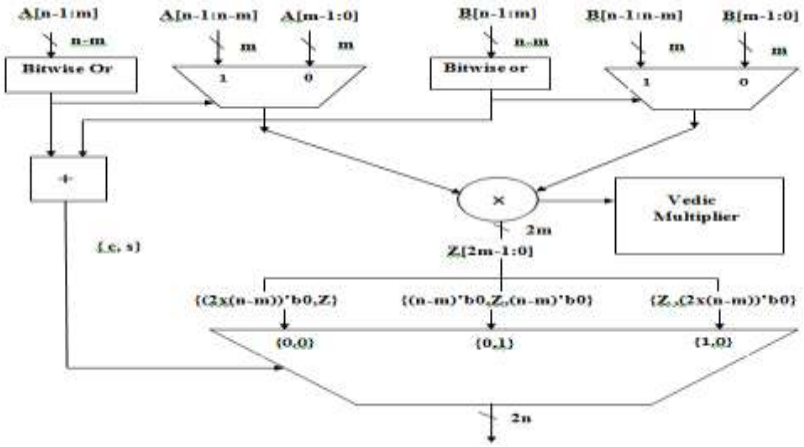

Fig 2: Approximate Multiplier Architecture using Static Segment Method

II. PROPOSED METHOD

In this approximate multiplier architecture, Vedic multiplier is replaced with Booth multiplier. In order to reduce the area and delay parameters compared to existing approximate architecture. The simulation and synthesis of both the architecture are checked by using Xilinx tool.

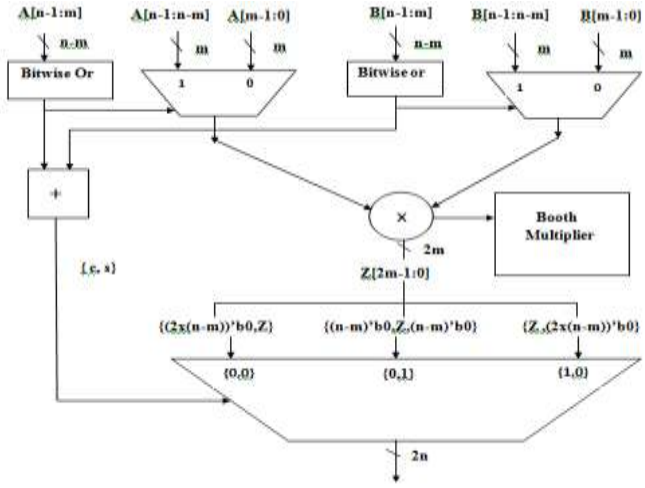

Fig 3 : Modified Approximate Multiplier Architecture using Static Segment Method

III. SYNTHESIS AND SIMULATION RESULTS

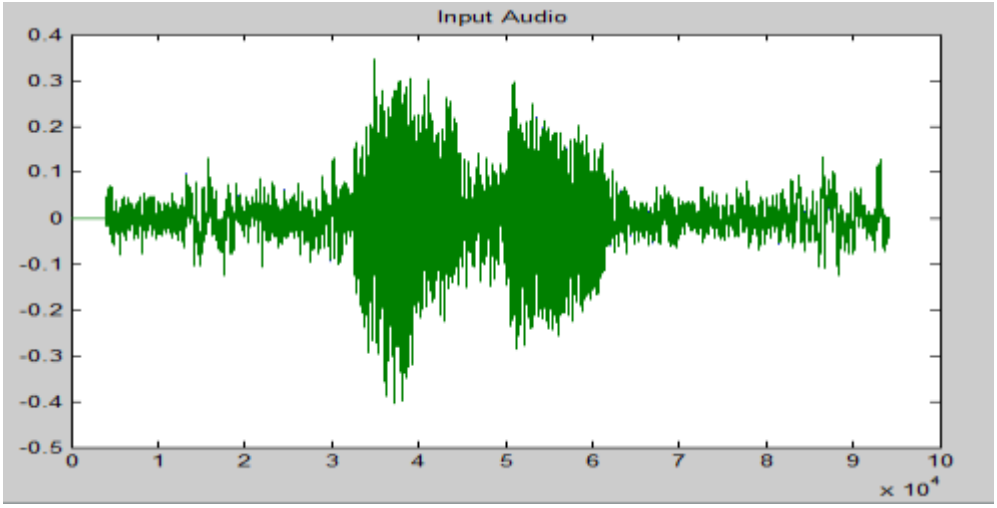

Fig 4 : Audio Signal of 2 sec

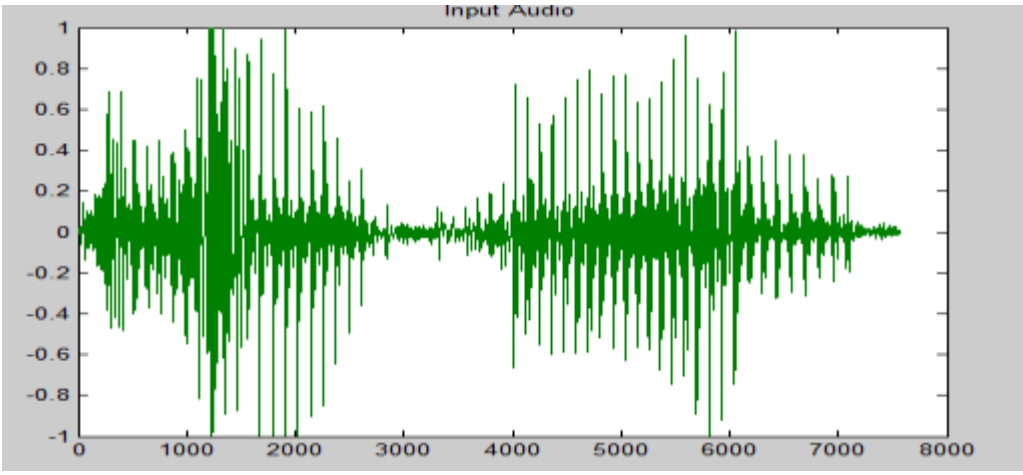

Fig 5: Audio Signal of 1sec

The binary data of these 2 audio signals is obtained by using Matlab tool .Considering a 2sec & 1sec as input and performs multiplication.

Fig 6 : Simulation Result of Approximate Multiplier Architecture using Static Segment Method

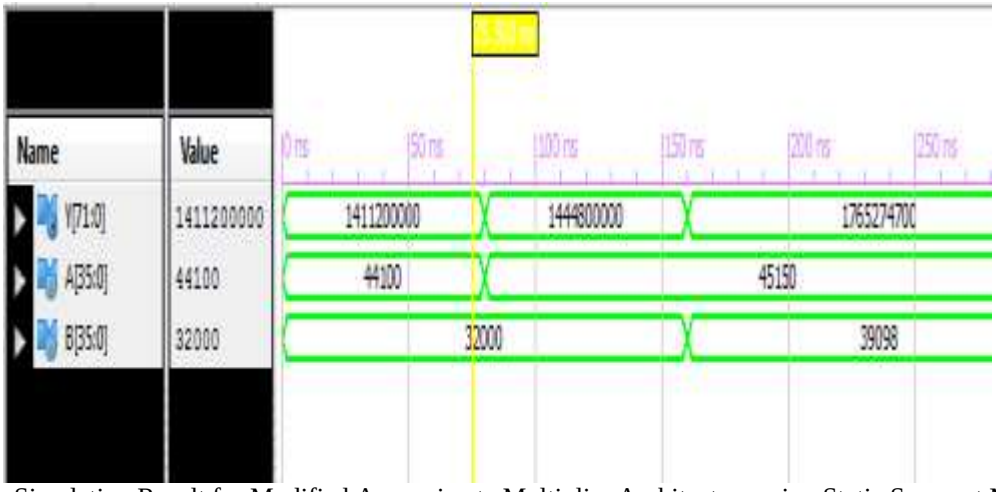

Fig 7: Simulation Result for Modified Approximate Multiplier Architecture using Static Segment Method

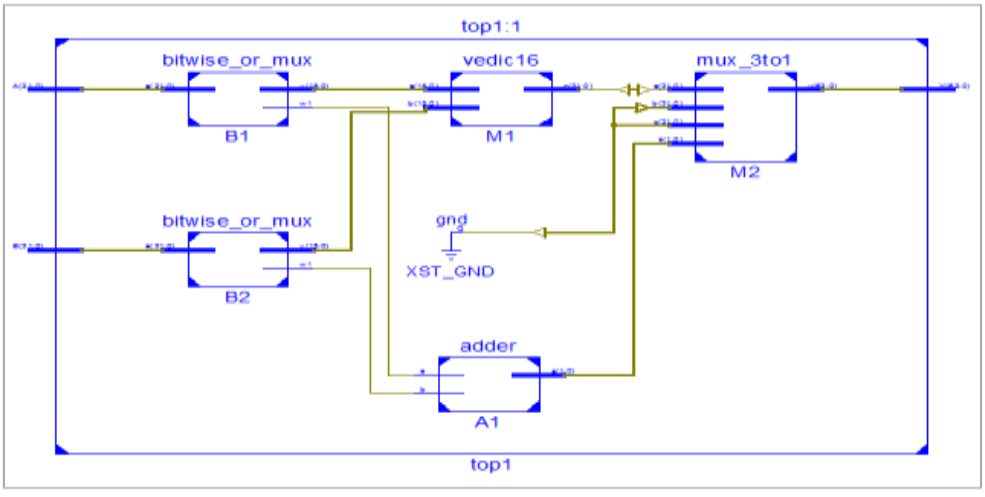

Fig 7 RTL Schematic for Approximate Multiplier using Static Segment Method

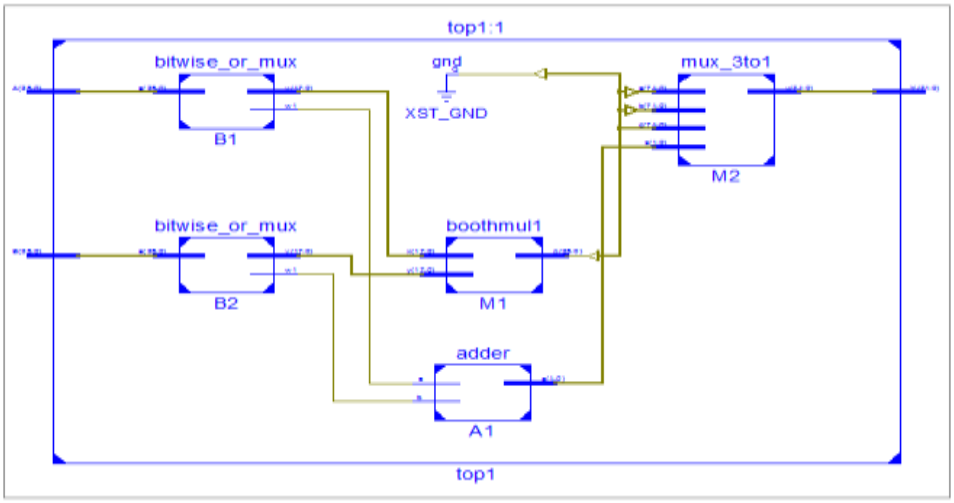

Fig 8 RTL Schematic for Modified Approximate Multiplier Architecture using Static Segment Method

IV. COMPARISIONS

Architectures /Parameters	Area (LUT's)	Delay
Existing method	1747	47.3ns
Proposed method	1596	37.3ns

V. CONCLUSION

In vlsi design the performance of any circuit depends on the factors area, power consumption and increased delay .In proposed architecture the area and delay are reduced compared to previous work at constant power consumption. The booth technology is adopted in this multiplier which makes the architecture faster. To improve the efficiency, the reduction of bits which are used to perform multiplication reduces the complexity of multiplication process. For various digital signal processing applications booth multiplier is used & also perform complex computations for various audio signals.

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