

Solar Based Binary Hybrid Cascaded Multilevel Inverter

K.Muthukumar¹, T.S.Anandhi²

^{*}(Department Of EIE, Annamalai University, Chidamabram, Tamilnadu India

^{**}(Department Of EIE, Annamalai University, Chidamabram, Tamilnadu India

ABSTRACT: The renewable energy especially photovoltaic system will be an increasingly important part of power generation. Day-by-day the energy demand is increasing and thus the needs for a solar energy are of prime importance. In this paper photovoltaic (PV) fed binary hybrid cascaded multilevel inverter (BHCMLI) is implemented using MATLAB/ Simulink. Maximum power point tracking (MPPT) algorithm is developed to improve the utilization efficiency of a photovoltaic systems. The proposed variable step size based incremental conductance MPPT algorithm is used to extract the maximum power from the PV panel. The multilevel inverter is controlled by multicarrier based sinusoidal pulse width modulation techniques with phase disposition (PD), phase opposition disposition (POD) and alternative phase opposition and disposition (APOD) PWM techniques. The different performance measures like V_{rms} , I_{rms} and total harmonic distortion (THD) are carried out using MATLAB/Simulink. The POD PWM provides a relatively low THD and higher fundamental RMS output voltage and current.

Keywords: Binary multilevel inverter. Buck converter. Incremental conductance. Photovoltaic. THD

I. INTRODUCTION

Photovoltaic's sources are used today in many applications such as battery charging, home power supply, water pumping and satellite power systems etc. Photovoltaic generation is becoming increasingly important as a renewable source since it is cost free, pollution free and noise free. PV modules still have relative low conversion efficiency due to always changing with weather conditions like solar irradiation and temperature [1]. To extract the maximum possible power from the PV module maximum power point tracking becomes significant. A very common offline MPPT techniques [2] are voltage and current based MPPT techniques which are not suitable for

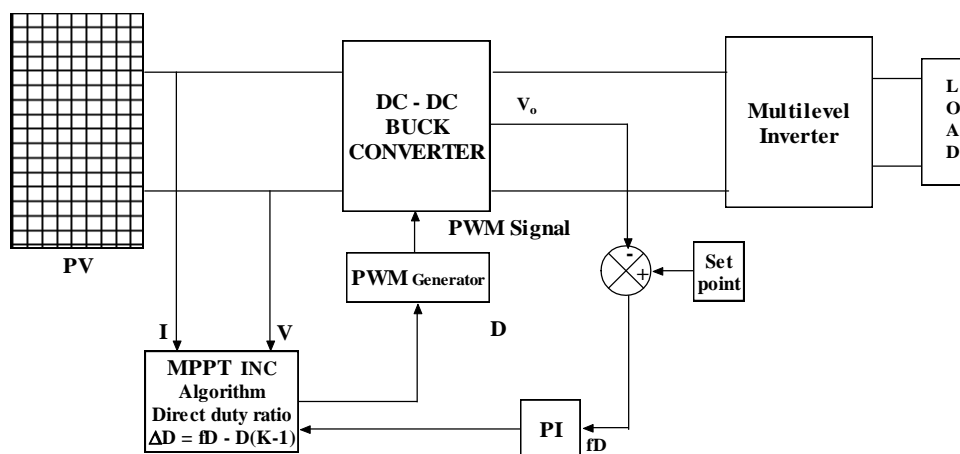


Figure 1 Block diagram of PV fed cascaded MLI

fast varying atmospheric conditions. Therefore online technique method perturb and observe (P&O) algorithm and incremental conductance algorithm (INC) are mostly preferred. In this paper variable step size based INC is proposed to extract the maximum power from the PV system. The buck converter is placed between the PV panel and multilevel inverter load. The developed PV model with MPPT and buck converter is fed as source to BHCMLI.

BHCMLI consists of two H-bridges. The H-bridges are fed from the PV panels of 12V and 24V each through a DC-DC converter. The 24V are obtained by connecting two PV panels in series. The overall block diagram of the system is shown in Figure 1. The cascaded MLI allows various pulse width modulation strategies [3] including selective harmonic elimination PWM (SHE-PWM), sinusoidal PWM (SPWM), space vector PWM (SVPWM) etc. In this paper the SPWM control method with a sinusoidal reference voltage waveform is compared with a triangular carrier wave form to generate switching gate signals are used

II. MATHEMATICAL MODEL OF A PV MODULE

A solar cell is a P-N semiconductor junction that converts solar energy into DC electrical energy. A solar cell exhibits a nonlinear I-V and P-V characteristics which vary with solar irradiation and cell temperature. Figure 2 shows the equivalent circuit model of a solar cell. The characteristics equation for this PV module is given by [4]

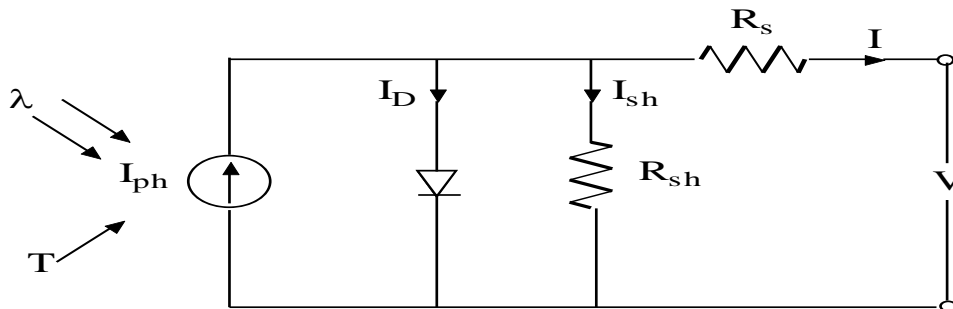


Figure 2 Equivalent circuit of a solar cell

Applying Kirchhoff's current law

$$I = I_{PH} - I_D - I_{SH} \tag{1}$$

$$I_D = I_S \left[\exp \left(q \left(\frac{V + IR_s}{k * A * T_C} \right) \right) \right] \tag{2}$$

$$I_{SH} = \frac{V + IR_s}{R_{sh}} \tag{3}$$

Substitute equation (2) and (3) in (1) we get

$$I = I_{PH} - I_S \left[\exp \left(\frac{q * (V + IR_s)}{k * A * T_C} \right) - 1 \right] - \frac{V + IR_s}{R_{sh}} \tag{4}$$

$$I_{PH} = [I_{SC} + K_I (T_C - T_{Ref})] \lambda / 1000 \tag{5}$$

$$K_I = \frac{I_{SC(T_2)} - I_{SC(T_1)}}{T_2 - T_1} \tag{6}$$

$$I_S = I_{RS} \left(\frac{T_C}{T_{Ref}} \right)^3 \left[\exp \left[\left(\frac{q * E_G}{k * A} \right) \left(\frac{1}{T_{Ref}} - \frac{1}{T_C} \right) \right] \right] \tag{7}$$

$$I_{RS} = \frac{I_{SC}}{\left[\exp \left(\frac{q * V_{OC}}{N_s * k * A * T_C} \right) - 1 \right]} \tag{8}$$

$$I = N_p * I_{PH} - N_p * I_S \left[\exp \left(\frac{q * (V + IR_s)}{N_s * k * A * T_C} \right) - 1 \right] - \frac{V + IR_s}{R_{sh}} \tag{9}$$

where I_{PH} is a light generated current, I_D is the diode current and I_{SH} is the shunt current since a typical PV cell produces less than 2.5W at 0.58V approximately, the cells must be connected in series configuration on a module to produce enough high power and is represented in equation 9. I and V are the cell's output current

and voltage. I_S is the cell's saturation of dark current, I_{RS} is the cell's reverse saturation current, q ($=1.6 \times 10^{-19}$ C) electron charge, k ($=1.3805 \times 10^{-23}$ J/K) is a Boltzmann's constant, T_C cell's working temperature, T_{Ref} cell's reference temperature, A is an ideal factor (Si poly = 1.3) E_G (=1.1) band-gap energy, λ is the solar insolation in kW/m^2 , where I_{SC} cell's short-circuit current at a 25°C and 1kW/m^2 , K_I is the cell's short-circuit current temperature coefficient, V_{OC} is the open circuit voltage, R_{sh} is the shunt resistance, R_s is the series resistance, N_s number of series cells and N_p number of parallel cell. The R_s and R_{sh} are calculated [5] by iteration method. Equations 5 to 9 are modelled using MATLAB/Simulink. The model parameters are identified from the manufacturer's data specification of a KCP 12060 solar modules are under standard test conditions (STCs) which means solar irradiation of 1000W/m^2 and temperature of 25°C as shown in Table 1. The I-V and P-V curves of a solar cell under standard test conditions are shown in Figure 3.

Table 1 Data specification of KCP 12060 module

| Data specification | Rating |
|------------------------------------|---------|
| Open circuit voltage V_{OC} | 21.20 V |
| Short circuit current I_{SC} | 4.03 A |
| Voltage at maximum power V_{mp} | 17 V |
| Current at maximum power I_{mp} | 3.50 A |
| Rated power | 59.5 W |
| Number of cell's in series N_s | 36 |
| Number of cell's in parallel N_p | 1 |

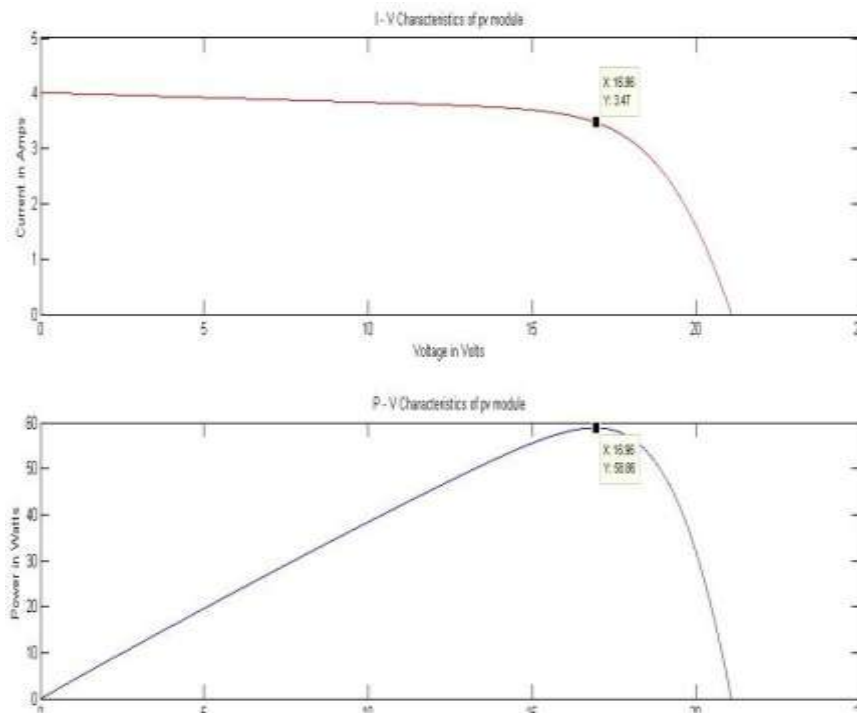


Figure 3 I-V and P-V characteristics of solar module at STCs

III. BUCK CONVERTER

DC-DC converters are used for converting one level of DC voltage to another regulated level of DC voltage. This DC transformation can be achieved by the circuit of storage elements like inductor, capacitor and the switching device used is a MOSFET. DC-DC converter is a high speed on/off semiconductor switch which connects source to load and disconnects the load from source at a high speed. A step-down converter produces an average output voltage, which is lower than the DC input voltage V_{in} . The basic schematic of a step-down converter is shown in Figure 4 In continuous-conduction mode of operation, assuming an MOSFET switch is on for the time duration t_{on} , the inductor current passes through the switch, and the diode becomes reverse biased. This results in a positive voltage across the inductor, which, in turn, causes a linear increase in the inductor current i_l . When the switch is turned off, because of the inductive energy storage, i_l continues to flow. This current flows through the diode and decreases. Average output voltage can be calculated in terms of the switch duty ratio as

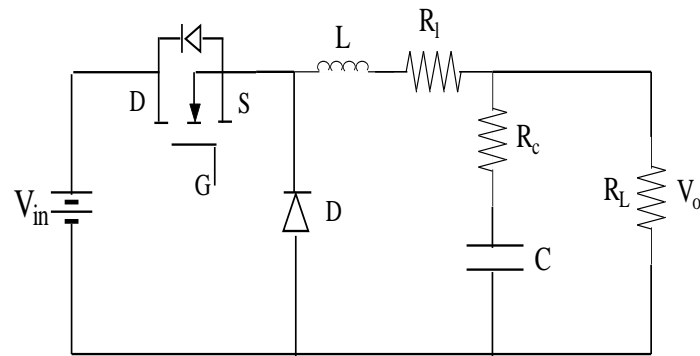


Figure 4 Buck converter

$$V_o = \frac{T_{on}}{T} V_{in} \quad (10)$$

$$D = \frac{T_{on}}{T} \quad (11)$$

$$V_o = D \times V_{in} \quad (12)$$

$$L = \frac{(V_{in} - V_o)D}{\Delta_{iL}f} \quad (13)$$

$$C = \frac{1-D}{8L \left(\frac{\Delta V_o}{V_o} \right) f^2} \quad (14)$$

where L is the inductance, V_{in} is the input voltage, V_o is the output voltage, D represents the duty cycle, f is the switching frequency and Δ_{iL} current ripple, ΔV_o is the ripple voltage and C is the capacitance the buck converter parameters values are shown in Table 2 and 3. The mathematical model of the buck converter can be derived [6] by the state space model to derive its transfer function which in turn tunes up the PID parameters to meet the transient and steady state specifications of the closed loop system. The process of adjusting the controller parameters [7] in order to meet the given performance specification is known as controller tuning. The most common Ziegler Nichols (ZN) tuning method is used in our work to obtain the controller parameters proportional gain K_c and integral time T_i .

Table 2 Specification of Buck converter 1 used by the first H-bridge

| Fs | Vin | V _o | L | C | R _L |
|-------|-----|----------------|------|------|----------------|
| 20Khz | 21V | 12V | 15mh | 10μF | 5Ω |

Table 3 Specification of Buck converter 2 used by the second H-bridge

| Fs | Vin | V _o | L | C | R _L |
|-------|-----|----------------|------|------|----------------|
| 20Khz | 42V | 24V | 25mh | 10μF | 10Ω |

IV. MAXIMUM POWER POINT TRACKING

When a solar module is used in a system, its operating point is decided by the load to which it is connected. The efficiency of PV system can be improved by the maximum power point tracking. The MPPT mechanism is based on the principle of impedance matching between load and PV module, which is necessary for maximum power transfer. The impedance matching is done by the DC to DC converter by changing the duty cycle of the switch. The perturb and observe and incremental conductance algorithm are online techniques [8]. The incremental conductance [INC] algorithm track the MPP at faster speed under varying atmospheric conditions than the P&O algorithm[9]. The principle of the INC algorithm is to increase or decrease the voltage by adjusting the duty cycle. The flow chart of the incremental conductance algorithm is shown in Figure 5. The increase and decrease of the duty cycle is based on the fixed step size ΔD . If ΔD chosen is small the response is sluggish and if ΔD chosen is large then the response is highly oscillatory. These disadvantages of fixed step size can be rectified by using a controller to vary the step size ΔD according to the response. These disadvantages

can be eliminated by means of a variable step size ΔD [10]. The step size can be adjusted automatically by means of a feedback PI controller hence PV system achieve more efficiency.

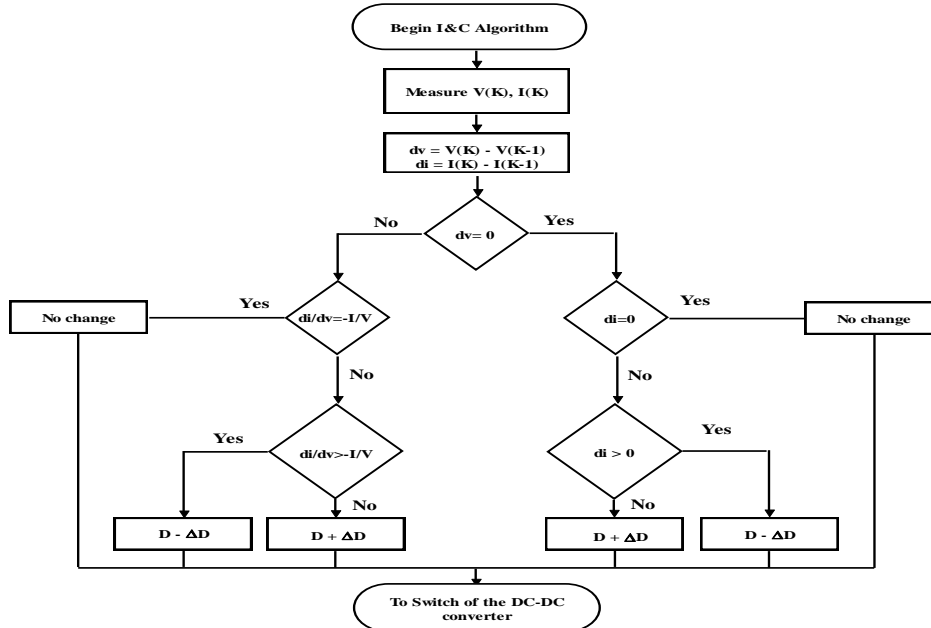


Figure 5 Flow chart of INC

V. BINARY HYBRID CASCADED MULTILEVEL INVERTER

Multilevel inverters offer high voltages from medium voltage dc sources and appear suitable for high power applications. Cascaded multilevel inverter is the popular topology and it does not require any clamping diodes or voltage balancing capacitors. The basic structure is based on the connection of H-bridges [HBs]. If the DC link voltages of HBs are identical then the multilevel inverter is called the symmetric multilevel inverter [11]. The quality of the output voltage is improved as the number of voltage level increases. Increase of the voltage levels by means combinations of the DC sources by binary/ trinary mode is called hybrid multilevel inverter [12]. Figure 6 shows the schematic of the single phase BHCMLI. The ratio of the DC link voltage is $1:2:\dots:2^{n-1}$ where n is the number of H – bridges. The maximum number of voltage level for 1Φ BHCMLI is 7 level [13]. E is considered as the unit DC link voltage and V_{dci} represents the DC link voltage of the i th H-bridge. In a 2H-bridges the DC link voltages are

$$V_{dci} = 2^{i-1} E \tag{15}$$

$$V_{dc1} = E \text{ and } V_{dc2} = 2E \tag{16}$$

In this paper V_{dc1} and V_{dc2} represents the solar fed buck converter with MPPT. Table 4 represents the switching pattern to generate 8 gating pulses in the required pattern to obtain 7 different levels of ac output voltage.

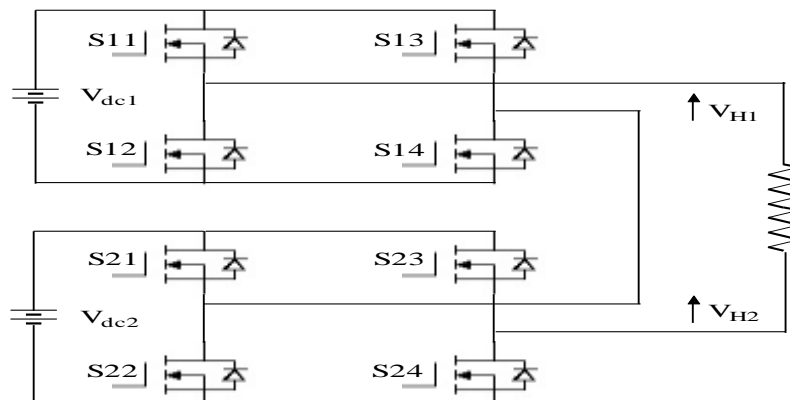


Figure 6 Binary hybrid cascaded multilevel inverter

Table 4 States of Switches in MLI

| S11 | S12 | S13 | S14 | S21 | S22 | S23 | S24 | V _{dc} |
|-----|-----|-----|-----|-----|-----|-----|-----|-------------------|
| ON | OFF | OFF | ON | ON | OFF | OFF | ON | +3V _{dc} |
| OFF | ON | OFF | ON | ON | OFF | OFF | ON | +2V _{dc} |
| ON | OFF | OFF | ON | OFF | ON | OFF | ON | +1V _{dc} |
| OFF | ON | OFF | ON | OFF | ON | OFF | ON | 0 |
| OFF | ON | ON | OFF | OFF | ON | OFF | ON | -1V _{dc} |
| OFF | ON | OFF | ON | OFF | ON | ON | OFF | -2V _{dc} |
| OFF | ON | ON | OFF | OFF | ON | ON | OFF | -3V _{dc} |

VI. MODULATION STRATEGIES FOR BHCMLI

Several modulation strategies have been developed for multilevel inverters. The most commonly used is the multi-carrier sub-harmonic PWM techniques [14]. The number of carriers required to produce the m level output is m-1. All the carriers have the same peak to peak amplitude. The sinusoidal reference is continuously compared with the triangular carrier signal and produces 1 if reference value is greater than the carrier value and zero otherwise. The frequency modulation index is

$$m_f = \frac{f_c}{f_r} \tag{17}$$

m_f is the frequency modulation, f_c is the carrier frequency and f_r is the reference frequency. The amplitude modulation for Phase Disposition (PD)/ Phase Opposition Disposition (POD)/ Alternative Phase Opposition Disposition APOD is

$$m_a = \frac{2A_r}{(m-1)*A_c} \tag{18}$$

where m_a represents the amplitude modulation A_r the reference amplitude and A_c the carrier amplitude. The different multi-carrier based MLI PWM strategies are developed using MATLAB-Simulink and uses 6 triangular carriers and bipolar sine wave reference signal. Figure 7 shows the reference signal and in – phase arrangement of carrier signals referred as PDPWM. Figure 8 shows that the reference signal and carrier signals arranged in – phase above zero reference and out - of phase below zero reference and hence referred as PODPWM. Figure 9 shows the alternate carrier signals which are out of phase / in phase with each other referred as APODPWM.

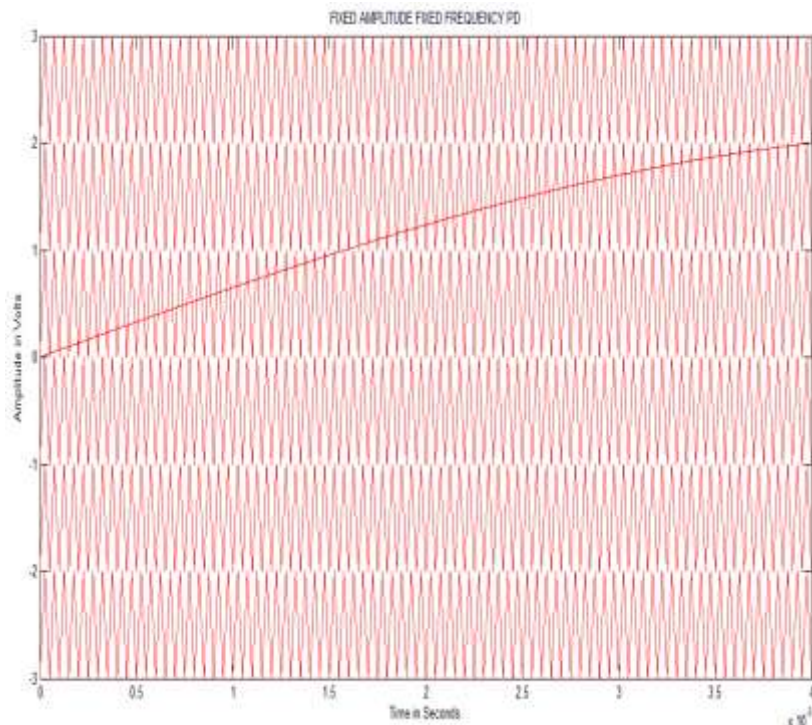


Figure 7 Carrier arrangements for PD PWM strategy m_a = 0.7, m_f = 400

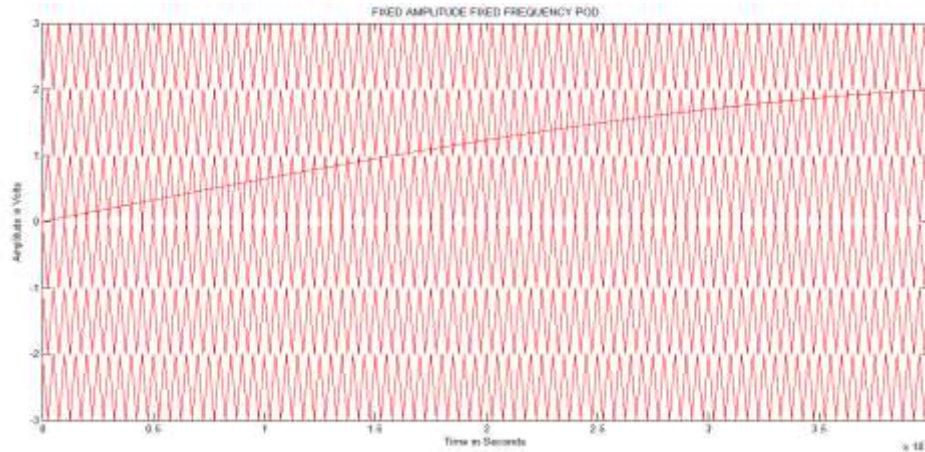


Figure 8 Carrier arrangements for POD PWM strategy $m_a = 0.7$, $m_f = 400$

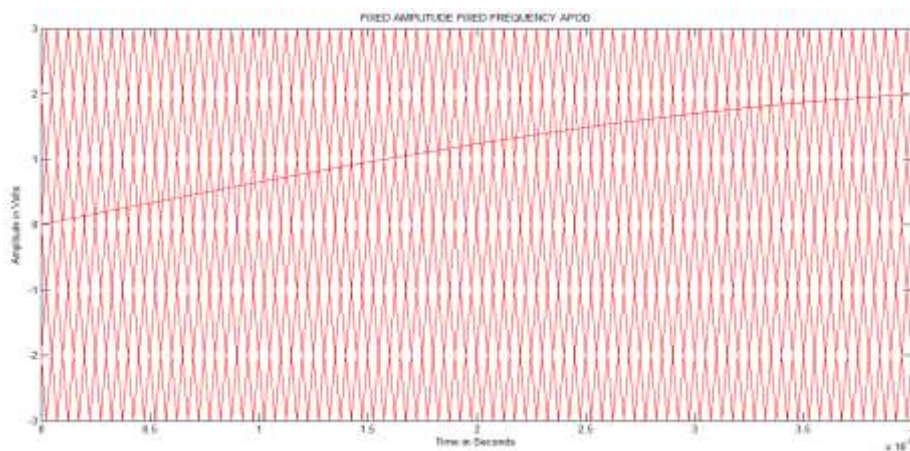


Figure 9 Carrier arrangements for APOD PWM strategy $m_a = 0.7$, $m_f = 400$

VII. SIMULATION RESULTS

The PV module, buck converter, variable step size based INC maximum power tracking and the binary hybrid cascaded multilevel inverter are developed and simulated using MATLAB/Simulink and the values are chosen as follows $V_{dc1}=12V$, $V_{dc2}=24V$ and $R_L=50\text{ohms}$ Figure 10 shows the different temperature and irradiation inputs to the solar panel. Figure 11 shows the first buck converter output 12V which is the source of the first H-bridge. The second buck converter output 24V and the input of the second H-bridge is shown in Figure 12. Figure 13, 15, and 17 shows the 7 level ac output voltage and current of the BHCMLI using PD, POD and APOD bipolar multicarrier PWM strategies respectively. The FFT analysis of 7 level output voltage and current of BHCMLI using PD, POD and APOD is shown in Figure 14, 16 and 18. Table 5 shows the performance measure V_{rms} , I_{rms} and %THD of 7 levels BHCMLI for different modulation index and POD method is found to perform better than PD and APOD methods.

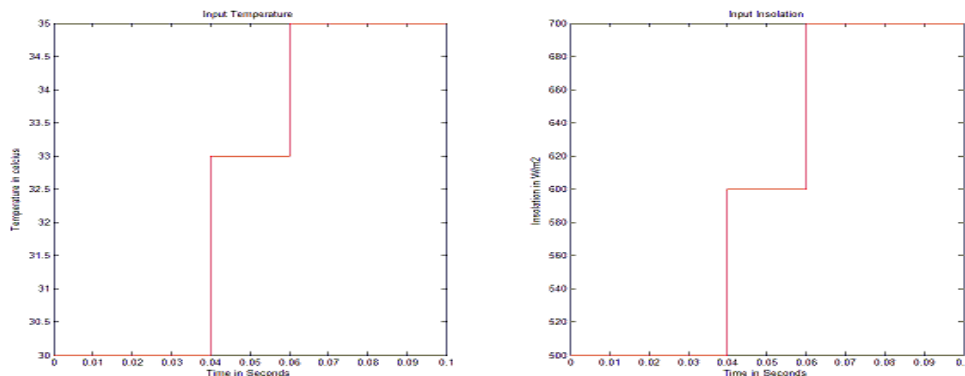


Figure 10 Variable temperature and irradiation input to solar panel

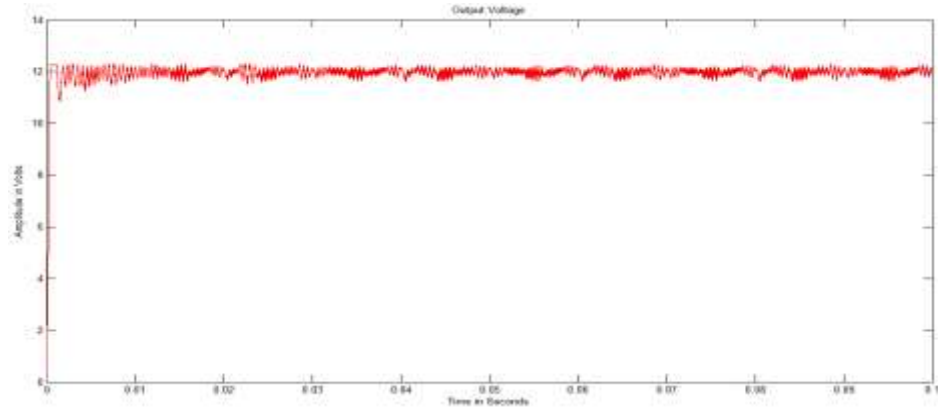


Figure 11 PV fed regulated voltage source of the first H-Bridge

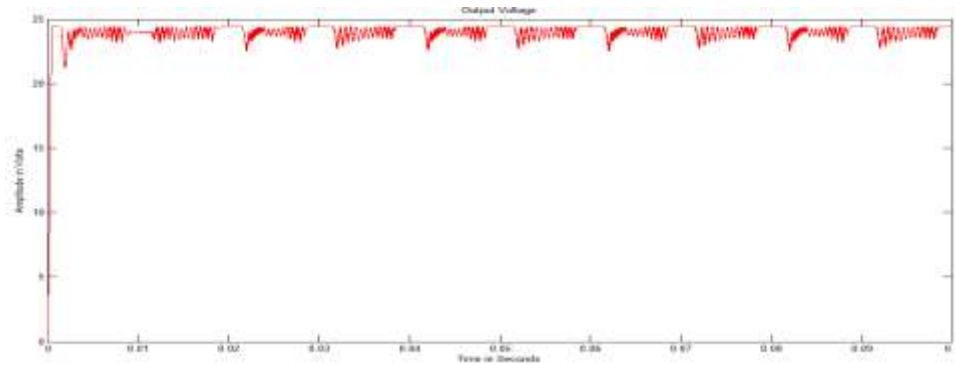


Figure 12 PV fed regulated voltage source of the second H-Bridge

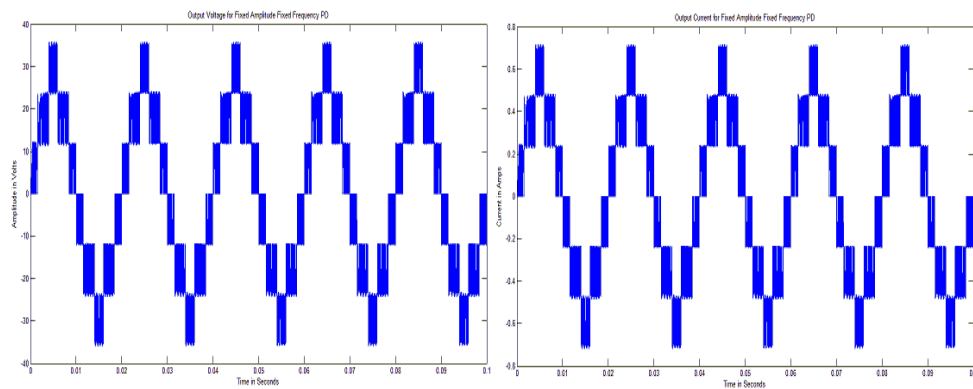


Figure 13 Seven level AC load voltage and current of BHCMLI using PD PWM

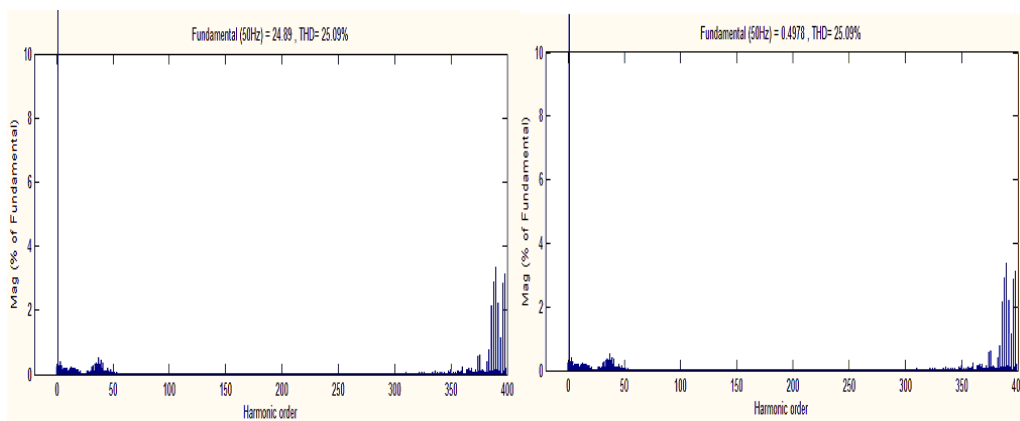


Figure 14 FFT analysis of 7 level output voltage and current of BHCMLI using PD PWM

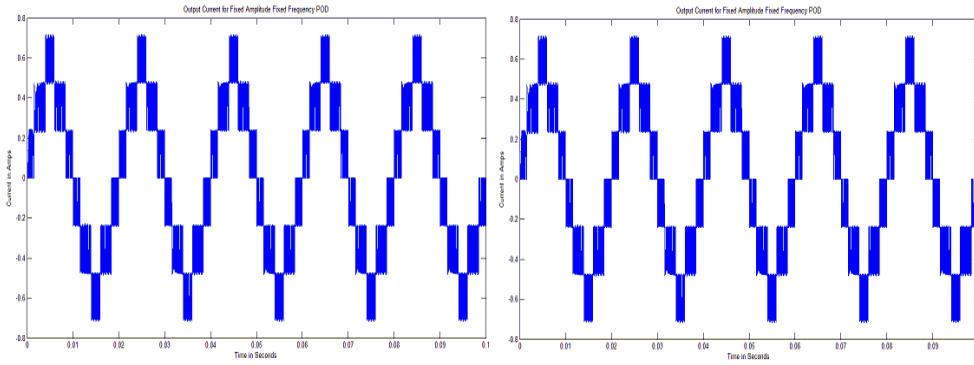


Figure 15 Seven level AC load voltage and current of BHCMLI using POD PWM

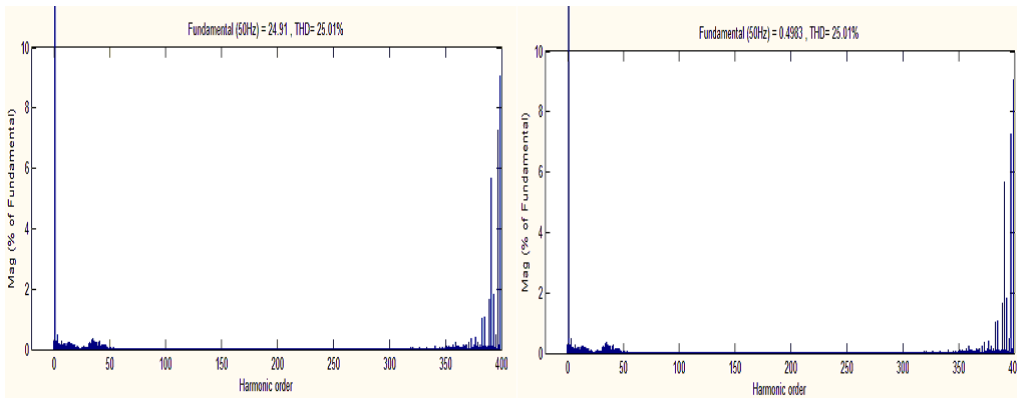


Figure 16 FFT analysis of 7 level output voltage and current of BHCMLI using POD PWM

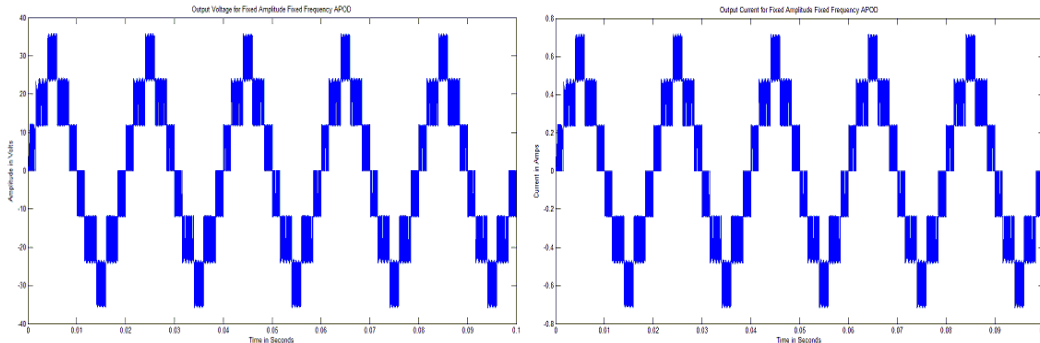


Figure 17 Seven level AC load voltage and current of BHCMLI using APOD PWM

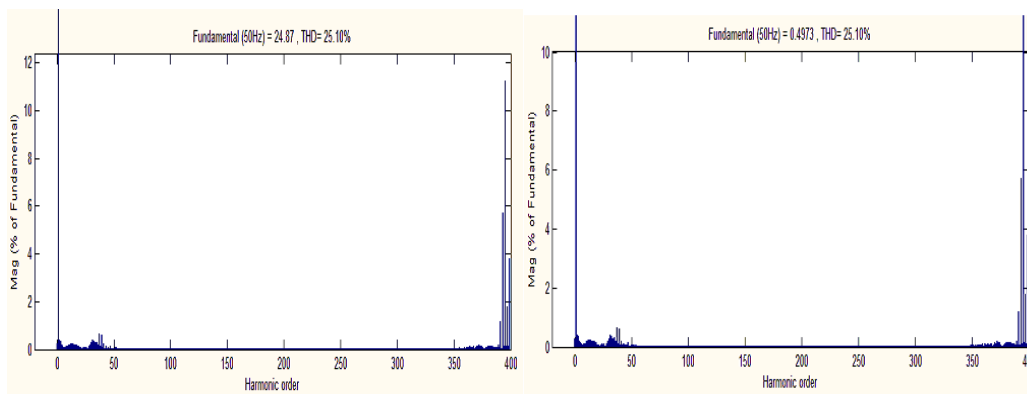


Figure 18 FFT analysis of 7 level output voltage and current of BHCMLI using APOD

Table 5 Performance evaluation of different parameters for 7 level BHCMLI

| ma | PD | | | POD | | | APOD | | |
|-----|------------|--------|-------|------------|--------|-------|------------|--------|-------|
| | Parameters | | | Parameters | | | Parameters | | |
| | Vrms | Irms | THD | Vrms | Irms | THD | Vrms | Irms | THD |
| 1.0 | 25.15 | 0.5031 | 17.87 | 25.17 | 0.5034 | 17.77 | 25.17 | 0.5033 | 17.88 |
| 0.9 | 22.65 | 0.4529 | 22.07 | 22.64 | 0.4529 | 21.98 | 22.63 | 0.4525 | 22.07 |
| 0.8 | 20.13 | 0.4025 | 23.96 | 20.13 | 0.4027 | 23.85 | 20.12 | 0.4023 | 23.97 |
| 0.7 | 17.6 | 0.352 | 25.09 | 17.62 | 0.3523 | 25.01 | 17.58 | 0.3517 | 25.10 |

VIII. CONCLUSION

The simulations results of solar based variable step size based incremental conductance algorithm based binary hybrid cascaded multilevel inverter are presented in this paper. To track the maximum power point tracking and better steady state voltage and current is achieved. The various multi carrier based PWM strategies such as PD, POD and APOD are performance evaluation analyzed for different parameters such as V_{rms} , I_{rms} and %THD for the 7 level BHCMLI. POD methods work satisfactory for better performance compared with PD and APOD methods.

ACKNOWLEDGEMENTS

The authors wish to thank Annamalai University for the constant support in the research process.

REFERENCES

- [1]. Eftichios Koutroulis, Kostas Kalaitzakis and Nicholas C. Voulgaris, Development of a microcontroller based photovoltaic maximum power point tracking control system, IEEE transactions on power electronics, vol. 16(1), 2001, 46-54.
- [2]. Pallavee Bhatnagar and R.K.Nema, Maximum power point tracking control techniques: State of the art in photovoltaic applications, Renewable and Sustainable Energy Reviews, 23, 2013, 224-241.
- [3]. Z. Jinghua, L. Zhengri, Research on hybrid modulation strategies based on general hybrid topology of multilevel inverters, proceedings of int symp power electronics, electric drives, motions, Italy, 2008.
- [4]. Huan-Liang Tsai, Ci-Siang Tu, and Yi-jie Su, Development of generalized photovoltaic model using MATLAB/SIMULINK, Proceedings of the world congress on engineering and computer science, 2008, 1-6.
- [5]. Marcelo Gradella villalva, Jonas Rafael Gazoli and Ernesto Ruppert Filho, Modelling and circuit-based simulation of photovoltaic arrays, Brazilian journal of power electronics, 14(1), 2009, 35-45.
- [6]. M.Natarajan and M.Yektaii, Modelling of DC-DC buck converters for large signal frequency response and limit cycles, IEEE transactions on circuits and systems, 53(8), 2006, 712-716.
- [7]. M.Namnabat, M.Bayatipoodeh and S.Eshtekardiha, Comparison the control methods in improvement the performance of the DC-DC converter, International conference on power electronics, 2007, 246-251.
- [8]. Mohamed A. Eltawil and Zhengming Zhao, MPPT techniques for photovoltaic applications, Renewable and sustainable energy reviews, 25, 2013, 793-813.
- [9]. Safari A, Mekhilef S, Simulation and hardware implementation of Incremental Conductance MPPT with Direct Control Method Using Cuk Converter, IEEE Transactions on Industrial Electronics, 58(4), 2010, 1154-1161.
- [10]. K.Muthukumar and T.S.Anandhi, Implementation of variable step based incremental conductance MPPT algorithm using dSPACE, International Journal of Applied Engineering Research, 10(24), 2015, 44357-44362.
- [11]. J. Rodriguez, J-S. Lai, FZ. Peng, Multilevel inverters: A survey of Topologies, Controls and Applications, IEEE Transactions on industrial electronics 49(4), 2002, 724 – 738.
- [12]. D.Ruiz-Caballero, L.Martinez, R.A.Reynaldo, S.A.Mussa, New asymmetrical hybrid multilevel voltage inverter. Power Electronics Conference, Brazilian, 2009, 354 – 361.
- [13]. Krishna Kumar Gupta, Shailendra Jain, A multilevel Voltage Source Inverter (VSI) to maximize the number of levels in output waveform, Electrical Power and Energy Systems, 45, 2013, 376 -383
- [14]. B.P. McGrath and Holmes, Multicarrier PWM strategies for multilevel inverter, IEEE Transactions on industrial electronics, 49(4), 2002, 858-867.