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International
Journal
Of Modern Engineering Research (IJMER)

A New Two-Dimensional Analytical Model of Small Geometry GaAs MESFET

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ABSTRACT : *In this paper, a simple and exact analytical model for Small Geometry GaAs MESFET is developed to determine the potential distribution along the channel of the device. The model is based on the exact solution of two-dimensional Poisson's equation in the depletion region under the gate. Then the obtained model is used to study the channel potential and threshold voltage of the device. Using the analytical model, the effect of the device parameter and bias conditions on performance of the device is investigated. The obtained results are graphically exhibited and discussed. In order to verification of the analytical results, TCAD device simulator is used and good accordance is observed.*

Keywords: *Analytical Model, Channel Potential, GaAS MESFET, Threshold Voltage, TCAD simulation*

I. INTRODUCTION

The feasibility of a Gallium Arsenide (GaAs) field-effect transistor employing a Schottky barrier gate is demonstrated by Mead for the first time [1]. Due to the intrinsic high mobility of GaAs material, this transistor takes advantage of higher carrier velocity which offers less transition time and faster response of the device [2]. Moreover, semi-insulating GaAs substrates decreases parasitic capacitances and simplifies the fabrication process. Also due to the absence of gate oxide layer, the MESFET device are naturally immune to oxide-related problems like radiation plasma damages and hot-carrier effects. Noise immunity, high thermal conductivity, and gain performance at microwave frequency are another outstanding features of this device [3]. Nowadays, GaAs MESFET's have gained a valuable place in the microwave communication, wireless data transfer (Wi-Fi) and high-speed microelectronic applications. Currently, GaAs based amplifiers, oscillators, mixers, switches, attenuators, modulators, and limiters are widely used in high-speed and high-density integrated circuits [4].

Evaluation of channel potential is one of the most essential necessities for analysis of MOS transistors. In this paper, we present an analytical model for Small Geometry GaAs MESFET by solving the two dimensional (2D) Poisson's equation. The model is used to compute the surface potential distribution in the active channel under the gate to explain the performance of the device.

In order to solve Poisson's equation we used the superposition method [5] and represent the resultant solution of 2-D Poisson's equations as the sum of the one-dimensional (1-D) and two-dimensional 2-D potential solutions. Regarding to the obtained results, we show that the presented analytical model can be used as an effective tool for design and characterization of high-performance small geometry GaAs MESFET including the short channel effects and the effect of alteration in device parameters and bias conditions. The correctness of the model is shown by comparing the model results with the 2D simulation results attained using ATLAS.

II. DEVELOPMENT OF THE ANALYTICAL MODEL

Fig. 1 illustrates a typical cross-sectional view of a small geometry GaAs MESFET under consideration, where x and y indicate the lateral and perpendicular directions to the channel length.

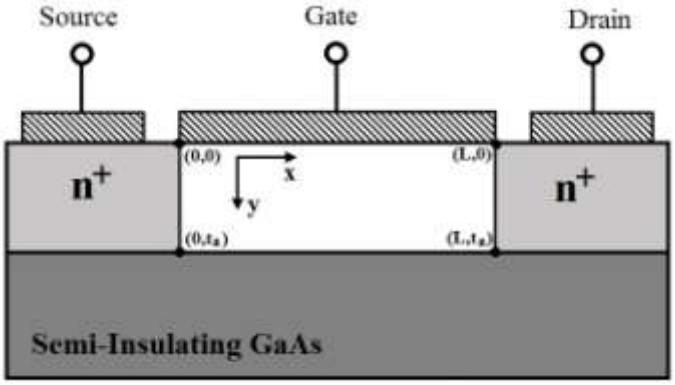

Fig. 1. The schematic view for GaAs MESFET structure

The primary desire part of the structure is the fully depleted region, the rectangular region under the Schottky gate. In general, the potential distribution in this region for the small geometry device can be represented by 2-D Poisson's equation in this region.

$$\frac{\partial^2 \Psi(x,y)}{\partial x^2} + \frac{\partial^2 \Psi(x,y)}{\partial y^2} = \frac{-qN_D}{\varepsilon_s} \qquad 0 \le x \le L \ , \ 0 \le y \le t_a \ (1)$$

where Ψ(x,y) is the electrostatic potential at any point of the active area , q is the charge of electron, ε_s is the dielectric constant of GaAs, N_D is the doping concentration, L is the gate length, and t_a is the thickness of the active layer.

To solve the Eq. (1), we make use of four boundary conditions as follow:

(A) Potential at the source end is

$$\Psi(x,y)\big|_{x=0} = \Phi_{bi} \ (2)$$

(B) Potential at the drain end is

$$\Psi(x,y)\big|_{x=L} = \Phi_{bi} + V_{DS} \ (3)$$

(C) Potential at top of the active channel is

$$\Psi(x,y)\big|_{y=0} = \Phi_{bi} - V_{GS} \ (4)$$

(D) Electric field in the bottom side of the active channel is

$$\frac{d}{dy}\Psi(x,y)\big|_{y=t_a} = 0 \ (5)$$

Where Φ_{bi} is the Schottky barrier built-in potential, V_{GS} is the applied gate-source voltage, and V_{DS} is the applied drain-source voltage.

In order to solve Poisson's equation we follow the technique proposed by Imam [6] for MOSFET's. In this technique, superposition method is used to decompose the 2-D Poisson's equation as the sum of the 1-D and 2-D potential solutions. The following equations express this method mathematically:

$$\Psi(x,y) = V(y) + U(x,y) \ (6)$$

where V(y) is the 1-D solution of the Poisson's equation in the direction along x-axis at a depth y which accounts for the long-channel effects.

$$\frac{d^2 V(y)}{dy} = \frac{-qN_D}{\varepsilon_s} \qquad 0 \le y \le t_a \ (7)$$

U(x,y) is the solution which accounts for the 2-D short-channel effects. Regarding to (1), (6), and (7), U(x,y) must satisfy the Laplace's equation:

$$\frac{\partial^2 U(x,y)}{\partial x^2} + \frac{\partial^2 U(x,y)}{\partial y^2} = 0 \quad 0 \le x \le L \ , \ 0 \le y \le t_a \ (8)$$

Regarding to Eq. (6), the boundary conditions defined for Ψ(x,y) are also separated into two proper parts. On doing so, the resulting boundary conditions for V(y) are derived from(4), and (5) as:

$$V(y)\big|_{y=0} = \Phi_{bi} - V_{GS} \quad (9)$$

$$\frac{d}{dy}V(y)\big|_{y=t_a} = 0 \quad (10)$$

Using boundary conditions (9) and (10), the solution of 1-D Poisson's equation is fined as

$$V(y) = \frac{-qN_D}{2\varepsilon_s}y^2 + \frac{qN_D t_a}{\varepsilon_s}y + \Phi_{bi} - V_{GS} \quad (11)$$

The resultant boundary conditions for U(x,y) are

$$U(x,y)\big|_{x=0} = \Phi_{bi} - V(y) \quad (12)$$

$$U(x,y)\big|_{x=L} = \Phi_{bi} + V_{DS} - V(y) \quad (13)$$

$$U(x,y)\big|_{y=0} = 0 \quad (14)$$

$$\frac{d}{dy}U(x,y)\big|_{y=t_a} = 0 \quad (15)$$

By using the standard technique of separation of variables method together with the boundary conditions of (12) –(15), the following resultant solution of the 2-D Laplace equation is found:

$$U(x,y) = \sum_{n=1}^{\infty}\left[A_n \sinh(k_n x) + B_n \sinh\left(k_n (L-x)\right)\right]\frac{\sin(k_n y)}{\sinh(k_n L)} \quad (16)$$

The parameter k_n and the Furrier series coefficients of A_n and B_n are described as

$$k_n = \frac{\pi}{2t_a} \quad (17)$$

$$A_n = \frac{f_n \cos(k_n t_a) + 2V_{GS}k_n^2\varepsilon_s - 2qN_D}{\varepsilon_s k_n^2\left[2k_n t_a - \sin(2k_n t_a)\right]} \quad (18)$$

$$B_n = \frac{(f_n - 2\varepsilon_s V_{DS})\cos(k_n t_a) + 2(V_{GS}+V_{DS})k_n^2\varepsilon_s - 2qN_D}{\varepsilon_s k_n^2\left[2k_n t_a - \sin(2k_n t_a)\right]} \quad (19)$$

where

$$f_n = qN_D\left(2 + k_n^2 t_a^2\right) - 2\varepsilon_s V_{GS} \quad (20)$$

Eventually, the resulting expression for Ψ(x,y) is

$$\Psi(x,y) = \frac{-qN_D}{2\varepsilon_s}y^2 + \frac{qN_D t_a}{\varepsilon_s}y + \Phi_{bi} - V_{GS} + \sum_{n=1}^{\infty}\left[A_n \sinh(k_n x) + B_n \sinh\left(k_n (L-x)\right)\right]\frac{\sin(k_n y)}{\sinh(k_n L)} \quad (21)$$

The next step is to obtain a model for threshold voltage. The threshold voltage can be defined as the gate voltage which achieves the minimum potential to preserve the fully depleted channel region [7]. Accordingly, the formation of the channel barrier can be used as a criterion to define the threshold voltage. From this point of view, for V_{DS}=0, we can write:

$$\Phi_b = \Psi_{min} + V_{th} - \Phi_{bi} = \Phi_{bc} \quad (22)$$

Where Φ_b is the height of channel barrier, Ψ_{min} is the minimum surface potential in the x direction, V_{th} is the threshold voltage, and Φ_{bc} is the height of channel barrier in threshold condition.

Here, we need to find the minimum surface potential along the channel and its position. So we can write[8]:

$$\frac{d}{dx}\Psi(x,y)\Big|_{\substack{x=x_{min}\\y=t_a}} \quad (23)$$

Substituting (21) into (23) yields

$$\sum_{n=1}^{\infty} k_n \left[A_n \sinh\left(k_n x_{\min}\right) + B_n \sinh\left(k_n \left(L - x_{\min}\right)\right)\right] \frac{\sin\left(k_n t_a\right)}{\sinh\left(k_n L\right)} = 0 \quad (24)$$

Due to the rapid decay of the Fourier series coefficients, the first terms, A_1 and B_1, are enough to represent the entire Fourier series [9]. According to this, the x_{min} can be simply found as

$$x_{\min} = \frac{1}{2k_1} \ln\left[\frac{A_1 - B_1 e^{k_1 L}}{A_1 - B_1 e^{-k_1 L}}\right] \quad (25)$$

Due to the symmetry of the device in source and drain regions, for $V_{DS}=0$ we have $A_1=B_1$. Regarding to this and replacing (25) into (21) and(22), after some mathematical manipulation, we obtain

$$V_{th} = \Phi_{bi} - \frac{qN_D t_a^2}{2\varepsilon_s} - A_1 \operatorname{sech}\left(\frac{k_1 L}{2}\right) \quad (26)$$

III. RESULTS AND DISCUSSION

This section involves with the results obtained from the analytical model and the ATLAS [10] simulation results. Based on the expressions derived in Section II, the bottom channel potential and threshold voltage are calculated and plotted for various device parameters and bias conditions. In all figures, the solid lines are used to represent the analytical results and symbols are used for the simulation results. In our calculation, the following constants are considered: $\varepsilon_s=13.1\times8.85\times10^{-14}$ F/cm, $\Phi_{bi}=0.85$V, $N_D=5\times10^{17}$ cm^{-3}, and kT/q =26 mV. Fig. 2 shows the profile of electrostatic potential between source and drain Ψ(x,y) against normalized position along the channel for various gate lengths. As shown in the figure, the minimum potential is raised by decreasing of gate length. Also for short gate lengths, the potential barrier is considerably increased. Good agreement between analytical and simulation results is seen.

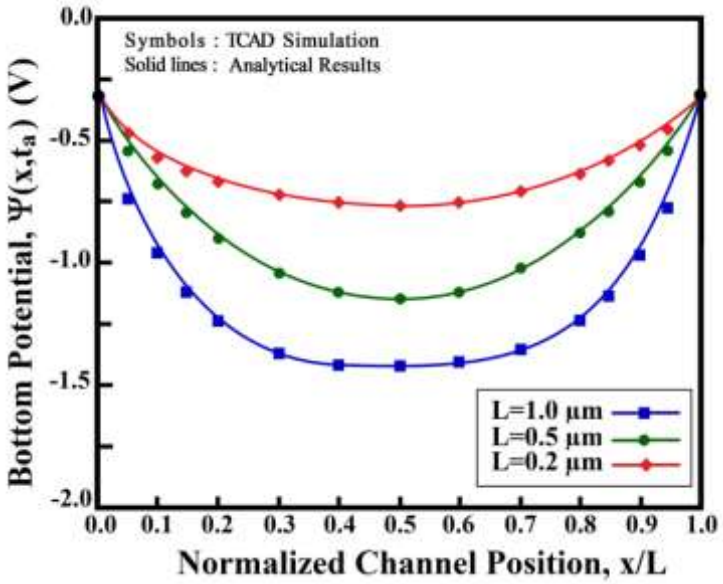

Fig. 2 The profile of bottom channel potential versus the position along the channel for various gate lengths.

The influence of drain bias on electrostatic potential is investigated in Fig. 3. It is clear from the figure that the minimum value of surface potential and its location depends on the drain voltage. This means that the potential barrier is lowered due to the drain bias. Fig. 4 shows the curve of channel potential distribution along the channel at different gate biases. As shown in the figure, the curve of potential is elevated with increasing of gate voltage.

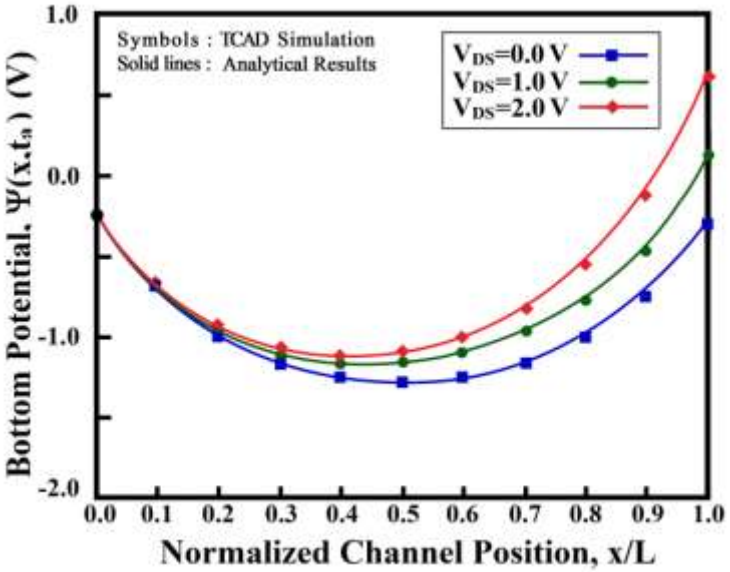

Fig. 3 The profile of bottom channel potential versus the position along the channel for various drain biases.

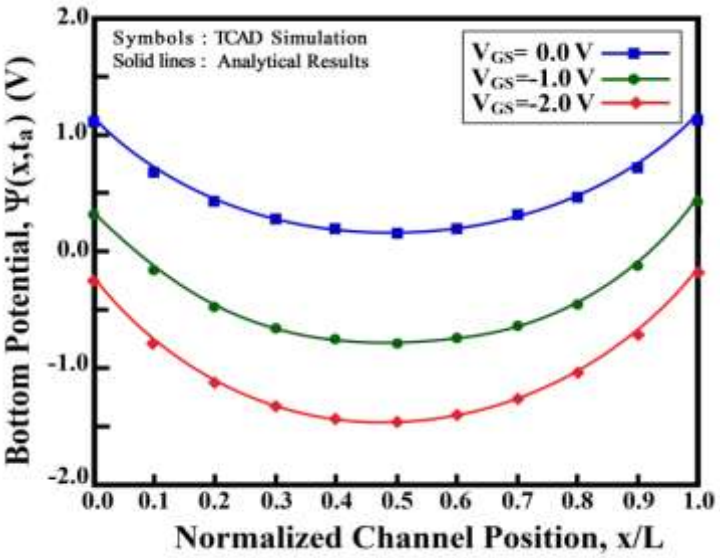

Fig. 4 The profile of bottom channel potential versus the position along the channel for various gate biases.

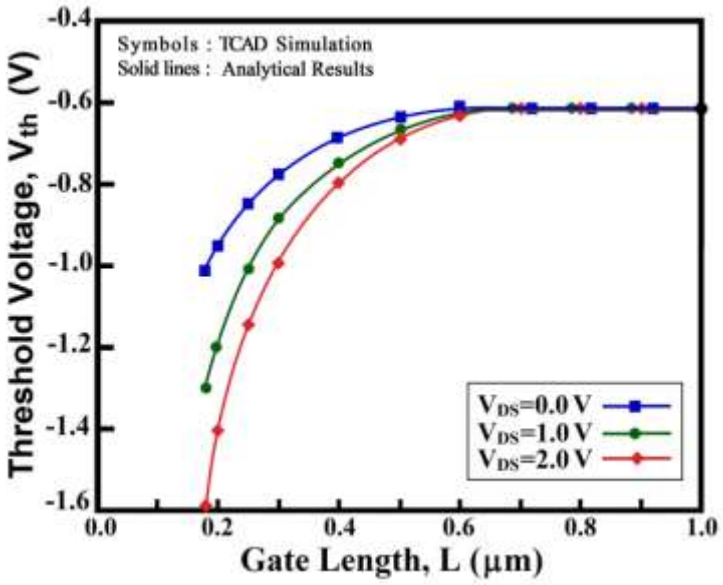

Fig. 5 The profile of threshold voltage versus the gate length for various drain biases.

In Fig. 5, the dependence of the threshold voltage on the channel length for three values of drain voltage is plotted. It is shown in this figure that the variation of threshold voltage versus drain voltage is negligible when gate length of device is long enough. For shorter gate devices, threshold voltage decreases little with increasing of drain voltage. Also the drain-induced threshold voltage roll-off behavior is shown very clearly. In Fig. 6, derived dependencies of the threshold voltage on the channel length for two values of active layer thicknesses is shown. According to the figure, the threshold voltage is considerably reduced as the thickness of active area is increased. In practice, the thickness of active layer cannot be reduced below a certain limit because tunneling will happens. Also it is observed that the threshold voltage calculated from the analytical model is close to the obtained simulation results. The effect of doping concentration on threshold voltage is investigated in Fig. 7. The threshold voltage is plotted against the channel length for two values of N_D. Figure shows that the threshold voltage decreases with increasing of N_D. Therefore, the device with higher doping concentration can be used for designing of low power circuits which need to the devices with low threshold voltage.

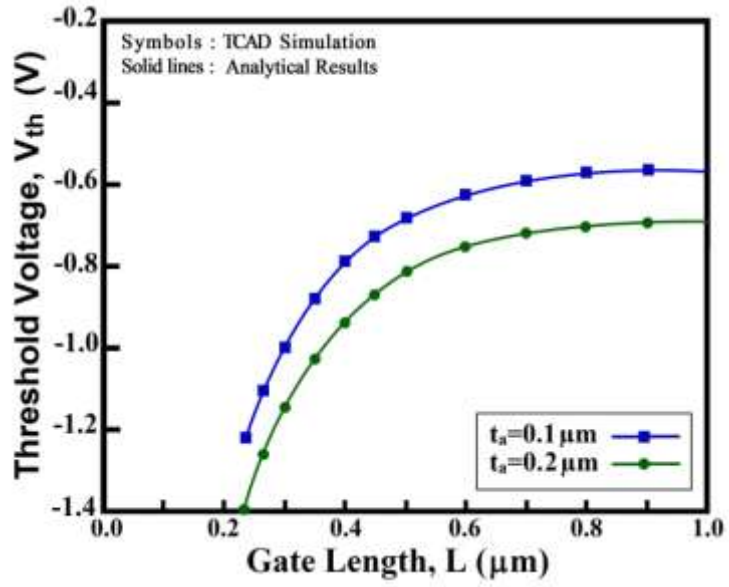

Fig. 6 The profile of threshold voltage versus the gate length for different thickness of active area.

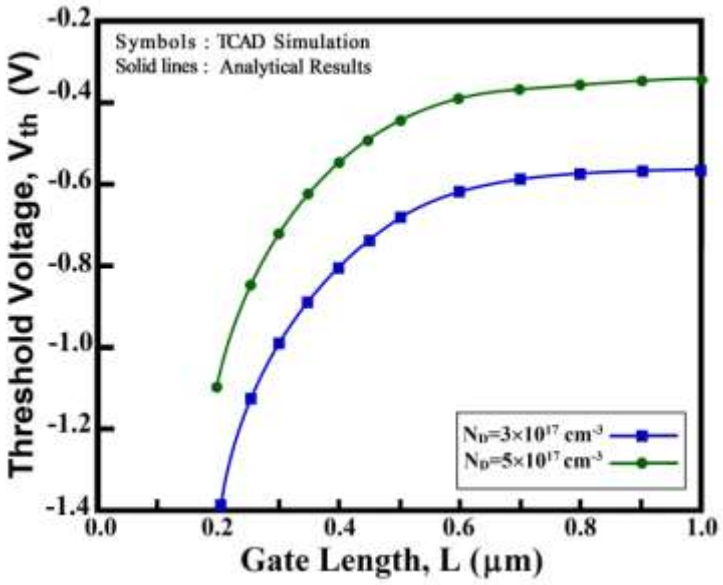

Fig. 7 The profile of threshold voltage versus the gate length for different channel concentration.

IV. CONCLUSION

In this paper, a simple analytical model for Small Geometry GaAs MESFET has been offered using the separation of variables method. The model predicts the variation of channel potential and threshold voltage upon device parameters like thickness of active layer and doping concentration. For validating the proposed analytical model, the 2-D device simulator ATLAS was used to simulate the channel potential in the silicon thin film and threshold voltage. The results obtained by the model are found to be in good accordance with ATLAS simulations.

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Hossein Mohammadi. " A New Two-Dimensional Analytical Model of Small Geometry GaAs MESFET." International Journal Of Modern Engineering Research (IJMER) 7.7 (2017): 72-78.