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Design and Simulation of Level Shifted Cascaded H-Bridge Multilevel Inverter Based DSTATCOM

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Abstract- This paper presents an investigation of five-Level Cascaded H – bridge (CHB) Inverter as Distribution Static Compensator (DSTATCOM) in Power System (PS) for compensation of reactive power and harmonics. The advantages of CHB inverter are low harmonic distortion, reduced number of switches and suppression of switching losses.The DSTATCOM helps to improve the power factor and eliminate the Total Harmonics Distortion (THD) drawn from a Non-Liner Diode Rectifier Load (NLDRL). The D-Q reference frame theory is used to generate the reference compensating currents for DSTATCOM while Proportional and Integral (PI) control is used for capacitor dc voltage regulation. A CHB Inverter is considered for shunt compensation of a 11 kV distribution system. Finally a level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) techniques are adopted to investigate the performance of CHB Inverter. The results are obtained through Matlab/Simulink software package.

Keywords- DSTATCOM, Level shifted Pulse width modulation (LSPWM), Phase shifted Pulse width modulation (PSPWM), Proportional-Integral (PI) control, CHB multilevel inverter, D-Q reference frame theory.

I. INTRODUCTION

Modern power systems are of complex networks, where hundreds of generating stations and thousands of load centers are interconnected through long power transmission and distribution networks. Even though the power generation is fairly reliable, the quality of power is not always so reliable. Power distribution system should provide with an uninterrupted flow of energy at smooth sinusoidal voltage at the contracted magnitude level and frequency to their customers. PS especially distribution systems, have numerous non linear loads, which significantly affect the quality of power. Apart from non linear loads, events like capacitor switching, motor starting and unusual faults could also inflict power quality (PQ) problems. PQ problem is defined as any manifested problem in voltage /current or leading to frequency deviations that result in failure or maloperation of customer equipment. Voltage sags and swells are among the many PQ problems the industrial processes have to face. Voltage sags are more severe. During the past few decades, power industries have proved that the adverse impacts on the PQ can be mitigated or avoided by conventional means, and that techniques using fast controlled force commutated power electronics (PE) are even more effective. PQ compensators can be categorized into two main types. One is shunt connected compensation device that effectively eliminates harmonics. The other is the series connected device, which has an edge over the shunt type for correcting the distorted system side voltages and voltage sags caused by power transmission system faults.

The STATCOM used in distribution systems is called DSTACOM (Distribution-STACOM) and its configuration is the same, but with small modifications. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage.

A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped, flying capacitor [2-5]. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges. This paper presents a DSTATCOM with a proportional integral controller based CHB multilevel inverter for the harmonics and reactive power mitigation of the nonlinear loads. This type of arrangements have been widely used for PQ applications due to increase in the number of voltage levels, low switching losses, low electromagnetic compatibility for hybrid filters and higher order harmonic elimination.

II.DESIGN OF MULTILEVEL BASED DSTATCOM

A. Principle of DSTATCOM

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure-1, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTATCOM and the ac system. Such

configuration allows the device to absorb or generate controllable active and reactive power.

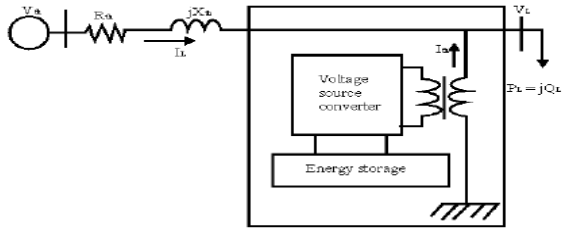

Figure – 1 Schematic Diagram of a DSTATCOM

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1. Voltage regulation and compensation of reactive power;
2. Correction of power factor
3. Elimination of current harmonics.

Here, such device is employed to provide continuous voltage regulation using an indirectly controlled converter. As shown in Figure-1 the shunt injected current I_{sh} corrects the voltage sag by adjusting the voltage drop across the system impedance Z_{th}. The value of I_{sh} can be controlled by adjusting the output voltage of the converter. The shunt injected current I_{sh} can be written as,

$$I_{sh} = I_L - I_S = I_L - (V_{th} - V_L) / Z_{th} \quad (1)$$

$$I_{sh} /\_\eta = I_L /\_- \theta \quad (2)$$

The complex power injection of the D-STATCOM can be expressed as,

$$S_{sh} = V_L I_{sh}^* \quad (3)$$

It may be mentioned that the effectiveness of the DSTATCOM in correcting voltage sag depends on the value of Z_{th} or fault level of the load bus. When the shunt injected current I_{sh} is kept in quadrature with V_L, the desired voltage correction can be achieved without injecting any active power into the system. On the other hand, when the value of I_{sh} is minimized, the same voltage correction can be achieved with minimum apparent power injection into the system.

B. Control for Reactive Power Compensation

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

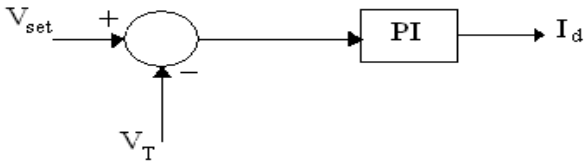

Figure-2 PI control for reactive power compensation

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the angle δ, which is provided to the PWM signal generator. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously. The PI controller processes the error signal and generates the required angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

C. Control for Harmonics Compensation

The Modified Synchronous Frame method is presented in [7]. It is called the instantaneous current component (i_d-i_q) method. This is similar to the Synchrous Reference Frame theory (SRF) method. The transformation angle is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the 3-phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. In the same way, the mains voltages $V_{(a,b,c)}$ and the available currents $i_{l\ (a,b,c)}$ in α-β components must be calculated as given by (4), where C is Clarke Transformation Matrix. However, the load current components are derived from a SRF based on the Park transformation, where 'θ' represents the instantaneous voltage vector angle (5).

$$\begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix} = [C] \begin{bmatrix} I_{la} \\ I_{lb} \\ I_{lc} \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} I_{ld} \\ I_{lq} \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix}, \theta = tan^{-1} \frac{V_\beta}{V_\alpha} \quad (5)$$

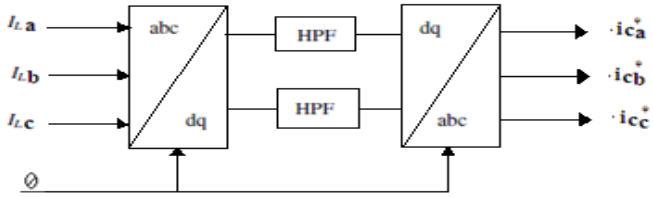

Figure-3 Block diagram of SRF method

Fig. 3 shows the block diagram SRF method. Under balanced and sinusoidal voltage conditions angle θ is a uniformly increasing function of time. This transformation angle is sensitive to voltage harmonics and unbalance; therefore dθ/dt may not be constant over a mains period.

With transformation given below the direct voltage component is

$$\begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha^2+V_\beta^2}} \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha^2+V_\beta^2}} \begin{bmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} \quad (7)$$

$$\begin{bmatrix} I_{Comp,a} \\ I_{Comp,b} \\ I_{Comp,c} \end{bmatrix} = [C]^T \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} \quad (8)$$

D. Cascaded H-Bridge Multilevel Inverter

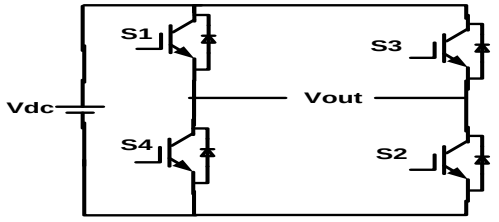

Figure-4 Circuit of the single cascaded H-Bridge Inverter

Fig.4 shows the circuit model of a single CHB inverter configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by 2n+1 and voltage step of each level is given by Vdc/2n, where n is number of H-bridges connected in cascaded. The switching table is given in Table 1.

Table-1 Switching table of single CHB inverter

Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

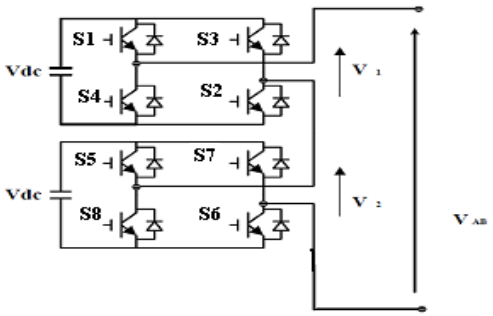

Figure-5 Block diagram of 5-level CHB inverter model

The switching mechanism for 5-level CHB inverter is shown in table-2.

Table 2. Switching table for 5-level CHB Inverter

Switches Turn On	Voltage Level
S1, S2	Vdc
S1,S2,S5,S6	2Vdc
S4,D2,S8,D6	0
S3,S4	-Vdc
S3,S4,S7,S8	-2Vdc

E. Design of Single H-Bridge Cell

1. Device Current

The IGBT and DIODE currents can be obtained from the load current by multiplying with the corresponding duty cycles. Duty cycle, d = ½(1+Kmsinωt), Where, m = modulation index K = +1 for IGBT, -1 for Diode. For a load current given by

$I_{ph} = \sqrt{2}\, I \sin(wt - \phi)$ (9)

Then the device current can be written as follows.

$$\therefore\ i_{device} = \frac{\sqrt{2}}{2} I \sin(wt - \emptyset) x\ (1 + km \sin wt) \quad (10)$$

The average value of the device current over a cycle is calculated as

$$i_{avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} \frac{\sqrt{2}}{2} I \sin(wt - \emptyset) x\ (1 + km \sin wt)\, dwt$$

$$= \sqrt{2I} \left[\frac{1}{2\pi} + \frac{k\,m}{g} \cos\varphi \right] \quad (11)$$

The device RMS current can be written as

$$i_{rms} = \sqrt{\int_{\varphi}^{\pi+\varphi} \frac{1}{2\pi} (\sqrt{2} I \sin(wt - \emptyset))^2\, x\, \frac{1}{2} x\, ((1 + km \sin wt)\, dwt)}$$

$$= \sqrt{2} I \sqrt{\frac{1}{g} + \frac{km}{3\pi} \cos\varphi} \quad (12)$$

B IGBT Loss Calculation

IGBT loss can be calculated by the sum of switching loss and conduction loss. The conduction loss can be calculated by,

$P_{on\,(IGBT)} = V_{ceo} * I_{avg\,(igbt)} + I^2_{rms\,(igbt)} * r_{ceo}$ (13)

$$I_{avg\ (igbt)} = \sqrt{2} I \left[\frac{1}{2\pi} + \frac{m}{g} cos\varphi \right] \quad (14)$$

$$I_{rms\ (igbt)} = \sqrt{2} I \sqrt{\left[\frac{1}{g} + \frac{m}{3\pi} cos\varphi \right]} \quad (15)$$

Values of V_{ceo} and r_{ceo} at any junction temperature can be obtained from the output characteristics (Ic vs. Vce) of the IGBT as shown in Fig .6.

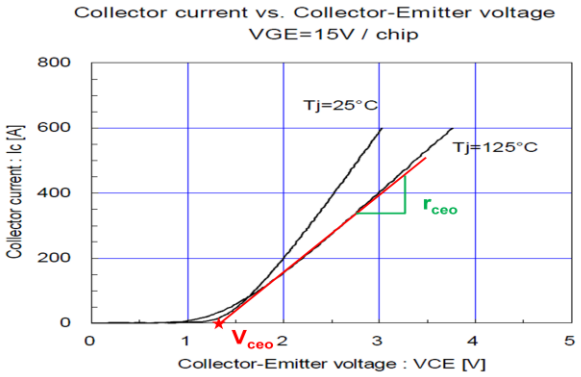

Figure 6 IGBT output characteristics

The switching losses are the sum of all turn-on and turn-off energies at the switching events

$$E_{sw} = E_{on} + E_{off} = a + bI + cI^2 \quad (16)$$

Assuming the linear dependence, switching energy

$$E_{sw} = (a + bI + cI^2) * \frac{V_{DC}}{V_{nom}} \quad (17)$$

Here V_{DC} is the actual DC-Link voltage and V_{nom} is the DC-Link Voltage at which E_{sw} is given. Switching losses are calculated by summing up the switching energies.

$$P_{sw} = \frac{1}{T_0}\Sigma_n E_{sw}(i) \quad (18)$$

Here 'n' depends on the switching frequency.

$$P_{sw} = \frac{1}{T_0}\Sigma_n (a + bI + cI^2) = \frac{1}{T_0}\left[\frac{a}{2} + \frac{bI}{\pi} + \frac{cI^2}{4}\right] \quad (19)$$

After considering the DC-Link voltage variations, switching losses of the IGBT can be written as follows.

$$P_{sw\,(IGBT)} = f_{sw}\left[\frac{a}{2} + \frac{bI}{\pi} + \frac{cI^2}{4}\right] * \frac{V_{DC}}{V_{nor}} \quad (20)$$

So, the sum of conduction and switching losses is the total losses given by

$$P_{T\,(IGBT)} = P_{on\,(IGBT)} + P_{sw\,(IGBT)} \quad (21)$$

C Diode Loss Calculation

The DIODE switching losses consist of its reverse recovery losses; the turn-on losses are negligible.

$$E_{rec} = a + bI + cI^2 \quad (22)$$

$$P_{sw\,(DIODE)} = f_{sw}\left[\frac{a}{2} + \frac{bI}{\pi} + \frac{cI^2}{4}\right] * \frac{V_{DC}}{V_{nor}} \quad (23)$$

So, the sum of conduction and switching losses gives the total DIODE looses.

$$P_{T\,(DIODE)} = P_{on\,(DIODE)} + P_{sw\,(DIODE)} \quad (24)$$

The total loss per one switch (IGBT+DIODE) is the sum of one IGBT and DIODE loss.

$$P_T = P_{T\,(IGBT)} + P_{sw\,(DIODE)} \quad (25)$$

D. Thermal Calculations

The junction temperatures of the IGBT and DIODE are calculated based on the device power losses and thermal resistances. The thermal resistance equivalent circuit for a module is shown in Fig 5. In this design the thermal calculations are started with heat sink temperature as the reference temperature. So, the case temperature from the model can be written as follows.

$$T_c = P_T R_{th\,(c\text{-}h)} + T_h \quad (26)$$

Here $R_{th(c\text{-}h)}$ = Thermal resistance between case and heat sink

P_T = Total Power Loss (IGBT + DIODE) (27)

IGBT junction temperature is the sum of the case temperature and temperature raise due to the power losses in the IGBT.

$$T_{j\,(IGBT)} = P_{T\,(IGBT)} R_{th\,(j\text{-}c)\,IGBT} + T_c \quad (28)$$

The DIODE junction temperature is the sum of the case temperature and temperature raise due to the power losses in the DIODE.

$$T_{j\,(DIODE)} = P_{T\,(DIODE)} R_{th\,(j\text{-}c)\,DIODE} + T_c \quad (29)$$

The above calculations are done based on the average power losses computed over a cycle. So, the corresponding thermal calculation gives the average junction temperature. In order to make the calculated values close to the actual values, transient temperature values are to be added to the average junction temperatures.

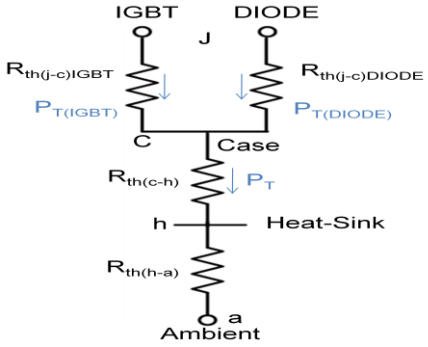

Figure. 5 Thermal resistance equivalent circuit

E. DC-Capacitor Selection

The required capacitance for each cell depends on the allowable ripple voltage and the load current. The rms ripple current flowing into the capacitor can be written as follows and the ripple current frequency is double the load current frequency.

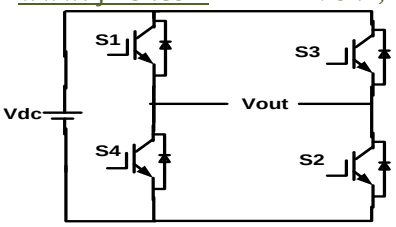

Fig. 6 H-Bridge converter

$$I_c = -\frac{1}{V_{dc}}\frac{1}{2}(|U_{ac}| * k + IwL)\sin(2wt) \quad (30)$$

Since the value of 'L' is very small, the above equation can be simplified to

$$I_c = -\frac{1}{V_{dc}}\frac{1}{2}(|U_{ac}| * k)\sin(2wt) \quad (31)$$

$$I_c = -k\frac{1}{2}\frac{|U_{ac}|}{V_{dc}} * \sin(2wt) = -k\frac{m}{2}\sin(2wt) \quad (32)$$

Here 'm' is the modulation index and

$I_{cp} = C\frac{du_{pp}}{dt}$; $\frac{m}{2}I\sqrt{2}$= C2w*ΔV V_{dc}

$$C = \frac{m}{4w}\frac{1}{\Delta V * V_{dc}}\sqrt{2}I \quad (33)$$

F. PWM Techniques for CHB Inverter

The most popular PWM techniques for CHB inverter are 1. Phase Shifted Carrier PWM (PSCPWM), 2. Level Shifted Carrier PWM (LSCPWM).

1. Phase Shifted Carrier PWM (PSCPWM)

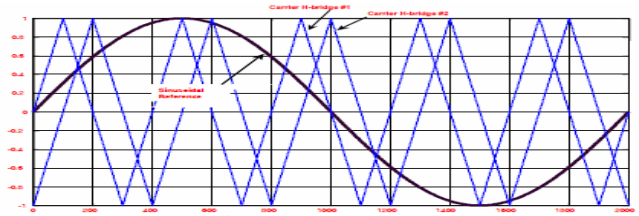
Fig. 7 phase shifted carrier PWM

Fig.7 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of 180°/m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

2. Level Shifted Carrier PWM (LSCPWM)

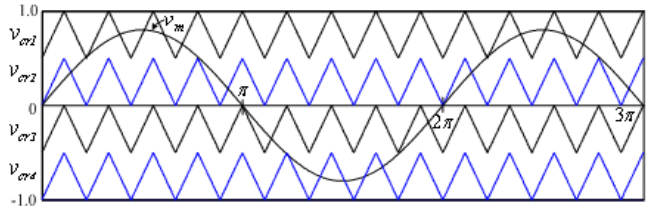

Fig. 8 Level shifted carrier PWM

Fig.8 shows the Level shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier Level shift by 1/m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

IV. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Fig. 9 shows the Matab/Simulink power circuit model of DSTATCOM. It consists of five blocks named as source block, non linear load block, control block, APF block and measurements block. The system parameters for simulation study are source voltage of 11kv, 50 hz AC supply, DC bus capacitance 1550e-6 F, Inverter series inductance 10 mH, Source resistance of 0.1 ohm and inductance of 0.9 mH. Load resistance and inductance are chosen as 30mH and 60 ohms respectively.

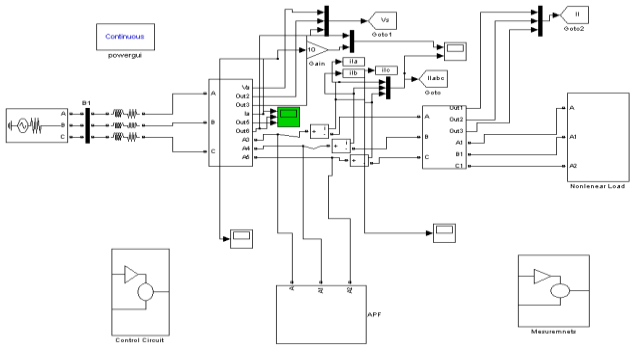
Fig. 9 Matlab/Simulink power circuit model of DSTATCOM

Fig. 10 shows the phase-A voltage of five level output of phase shifted carrier PWM inverter.

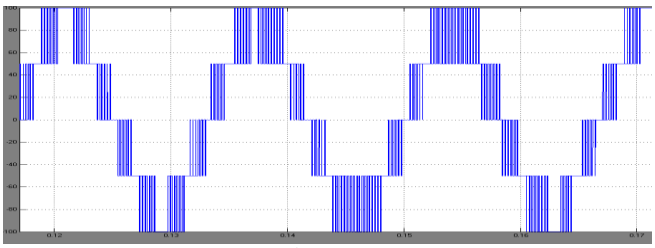
Fig. 10 five level PSCPWM output

Fig. 11 shows the three phase source voltages, three phase source currents and load currents respectively without DSTATCOM. It is clear that without DSTATCOM load current and source currents are same.

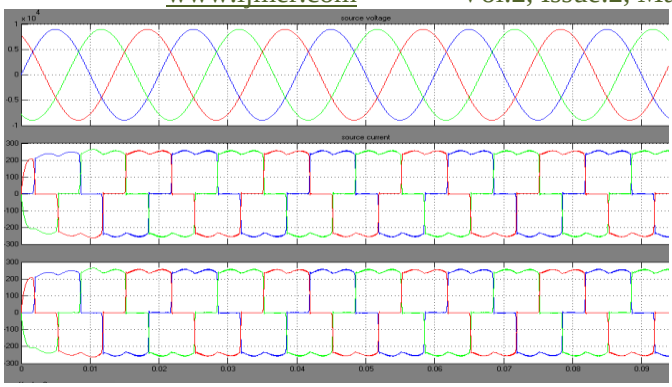

Fig. 11 Source voltage, current and load current without DSTATCOM

Fig. 12 shows the three phase source voltages, three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOM even though load current is non sinusoidal source currents are sinusoidal.

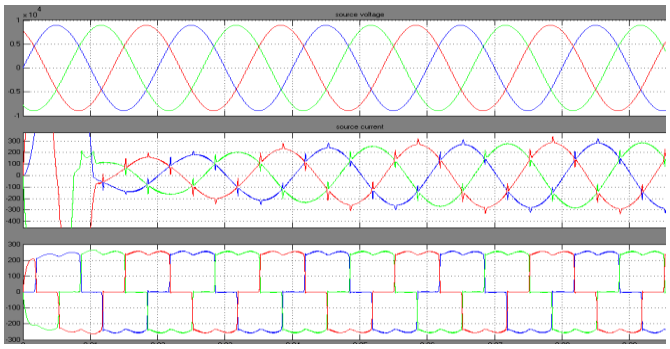

Fig. 12 Source voltage, current and load current with DSTATCOM

Fig. 13 shows the DC bus voltage. The DC bus voltage is regulated to 11kv by using PI regulator.

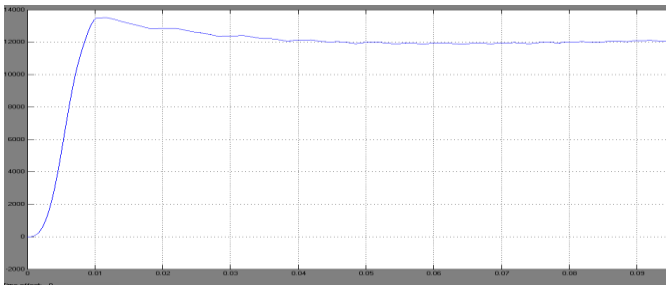

Fig. 13 DC Bus Vooltage

Fig. 14 shows the phase-A source voltage and current, even though the load is non linear RL load the source power factor is unity.

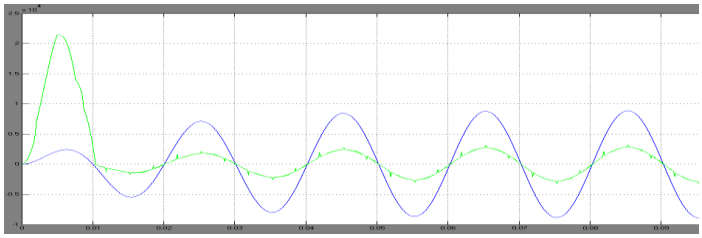

Fig. 14 Phase-A source voltage and current

Fig. 15 shows the harmonic spectrum of Phase –A Source current without DSTATCOM. The THD of source current without DSTACOM is 36.89%.

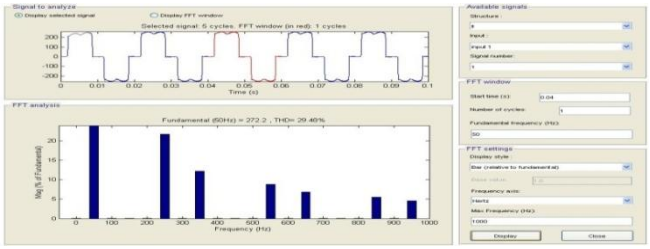

Fig. 15 Harmonic spectrum of Phase-A Source current without DSTATCOM

Fig. 16 shows the harmonic spectrum of Phase –A Source current with DSTATCOM. The THD of source current without DSTACOM is 5.05%

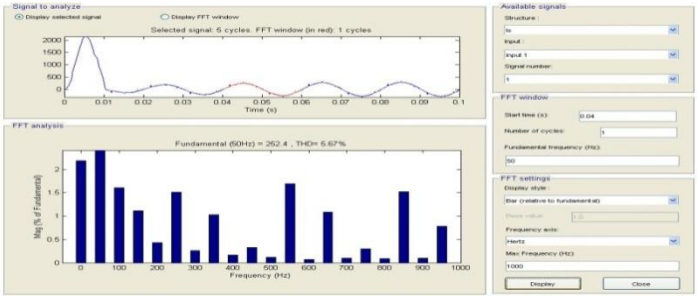

Fig. 16 Harmonic spectrum of Phase-A Source current with DSTATCOM

VI. CONCLUSION

A DSTATCOM with five level CHB inverter is investigated. Mathematical model for single H-Bridge inverter is developed which can be extended to multi H-Bridge. The source voltage , load voltage , source current, load current, power factor simulation results under non-linear loads are presented. Finally Matlab/Simulink based model is developed and simulation results are presented.

References

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