International Journal of Modern Engineering Research (IJMER)

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1086-1091 ISSN: 2249-6645

The Comparative THD Analysis of Neutral Clamped Multilevel Z-Source Inverter using Novel PWM Control Techniques

S. Mohamed Yousuf[1], P. Vijayadeepan[2], Dr. S. Latha[3]

**Assistant Professor in EEE, Sri Subramanya College of Engg and Tech, Palani, T.N, India.*

***Assistant Professor in EEE, Sri Subramanya College of Engg and Tech, Palani, T.N, India.*

****Associate Professor in EEE, Thiagarajar College of Engg, Madurai, T.N, India.*

ABSTRACT

A multilevel inverter is a power electronic device made to synthesize a desired AC voltage from several levels of DC voltages. These types of inverters are suitable in various high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum and faithful output. Multilevel inverters through a single X-shaped LC impedance network is an important development in recent years. The power quality improvement is achieved by reducing the harmonics present at the output voltage of the inverter. The total harmonics distortion (THD) values of the output voltages of the inverter are measured and compared. This paper presents the comparative analysis of several multicarrier PWM techniques, which is effectively used for harmonic mitigation in the proposed neutral clamped multilevel Z-Source inverter and this work is compared with conventional three level inverter by using MATLAB-SIMULINK.

Key words: **Multi-Carrier PWM Control, Multilevel Inverter, Neutral Point Clamped (NPC) Inverter, Total Harmonic Distortion (THD), Z-Source Inverter.**

I. INTRODUCTION

In the recent years, the revolution of multilevel inverters has many attractive features. In particular, high voltage capability, reduced common mode voltages near sinusoidal outputs, lower value of dv/dt, smaller or even number output filters make multilevel inverter is a suitable topology for variable frequency induction motor drives and have recently been explored for low-voltage renewable grid interfacing applications[1], [5]. Despite of their generally favorable output performance, NPC inverters are constrained by their ability to perform only voltage-buck operation if no additional dc–dc boost stages are added to their front-ends. To overcome this limitation, a buck–boost Z-source NPC inverter is proposed in [1], [2]. An additional X-shaped impedance networks are added between two isolated dc sources and a neutral clamped circuitry, as illustrated in Fig. 1. The unique structure of the multilevel Z-source inverters allows them to reach high voltage with low harmonics without the use of transformers [8].

A zero harmonic distortion of the output wave can be obtained by an infinite number of levels. To synthesize multi level output ac voltage using different levels of dc inputs, semiconductors devices must be switched ON and OFF in such a way that desired fundamental is obtained with minimum harmonic distortion. There are different types of approaches for the selection of switching techniques for the multilevel inverters. The multilevel inverters are mainly controlled with sinusoidal PWM technique and the proposed inverter can reduce the harmonic contents by using multicarrier PWM technique arrangements [5]. The 3-level NPC inverter with Z-Source is discussed in the references [1], [2] and the same inverter along with various multicarrier PWM techniques is discussed in the references [3]-[6], [8], [10]. The 5-level NPC inverter with space vector modulation is discussed in the references [7], [11].

In this paper, various multicarrier PWM techniques like Phase disposition (PD), Phase opposition disposition (POD), Alternative phase opposition disposition (APOD), phase shifted (PS) are proposed for three phase five level neutral clamped multilevel Z-Source inverter and the total harmonic distortion (THD) analysis is done for different modulation schemes. The proposed inverter can reduce the harmonic contents in the output phase voltages significantly. The total harmonic distortion (THD) reduction performance of three phase five level neutral clamped multilevel Z-Source inverter by using multicarrier PWM techniques are presented and the proposed work is compared with conventional three level neutral clamped multilevel inverter.

II. DESIGN AND OPERATION OF NEUTRAL CLAMPED MULTILEVEL INVERTER

The neutral clamped inverter, also known as diode clamped inverter. The basic architecture of this inverter discussed in references [7], [11]. The neutral clamped inverter delivers the staircase output voltage using several levels of DC voltages developed by DC capacitors. If m is the number of level, then the number of capacitors required on the DC bus are (m-1), the number of power electronic switches per phase are 2(m-1) and the number of diodes per phase are 2(m-2). This design formula is most common for all the neutral clamped multilevel inverters. The DC bus voltage is split into three levels using two capacitors C_1 and C_2, for five levels using four capacitors C_1, C_2, C_3 and C_4 as shown in Fig .1 and Fig .2. The voltage across each capacitor is $V_{dc}/4$ and the voltage stress across each switch is limited to one capacitor voltage through clamping diodes. The switching sequences of three phase 3-level and 5-level neutral clamped multilevel inverter are shown in table. I and II. As the number of levels increase the harmonic distortion decreases and efficiency of the inverter increases because of the reduced switching losses. The number of levels in multilevel inverters is limited because of the large number of clamping diodes required. The reverse recovery of these diodes is especially with multicarrier PWM techniques in a high voltage application is a major design challenge.

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1086-1091 ISSN: 2249-6645

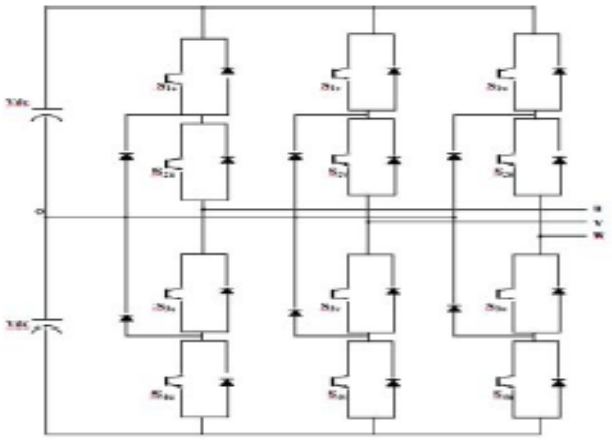

Fig .1. 3-Level Neutral Clamped Multilevel Inverter

TABLE I
THREE-LEVEL SWITCHING SEQUENCES

Terminal voltages	Switching Sequences			
	S_{a1}	S_{a2}	S_{a3}	S_{a4}
V_{DC}	on	on	off	off
o	off	on	on	off
$-V_{DC}$	off	off	on	on

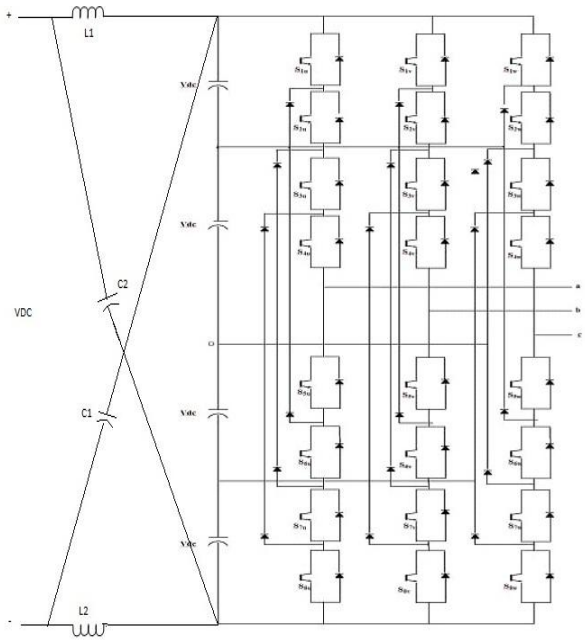

Fig .2. 5-Level Neutral Clamped Multilevel Inverter

TABLE II
FIVE-LEVEL SWITCHING SEQUENCES

Terminal voltages	Switching Sequences							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
$2V_{DC}$	on	on	on	on	off	off	off	off
V_{DC}	off	on	on	on	on	off	off	off
0	off	off	on	on	on	on	off	off
$-V_{DC}$	off	off	off	on	on	on	on	off
$-2V_{DC}$	off	off	off	off	on	on	on	on

III. CONTROL TECHNIQUES OF MULTILEVEL INVERTER

Multicarrier PWM Techniques involves the natural sampling of single modulating reference waveform typically being sinusoidal, through several carrier signals typically being triangular waveforms This modulation method is the logical extension of sine-triangle PWM for multilevel inverters, in which m-1 carriers are needed for m-level inverter. They are arranged in vertical shifts in continuous bands defined by the levels of the inverter. Each carrier has the same frequency and amplitude. A single voltage reference is compared to the carrier arrangement and the generated pulses are associated to each switching devices [6], [8].

A. Phase Disposition (PD)

This technique involves a number of carriers (m-l) which are all in phase accordingly. In 5 -level inverter all the four carrier waves are in phase with each other and compared with reference signal [4], [10]. According to that, the gate pulses are generated and are associated to each switching devices. The phase disposition PWM technique is illustrated in Fig. 3

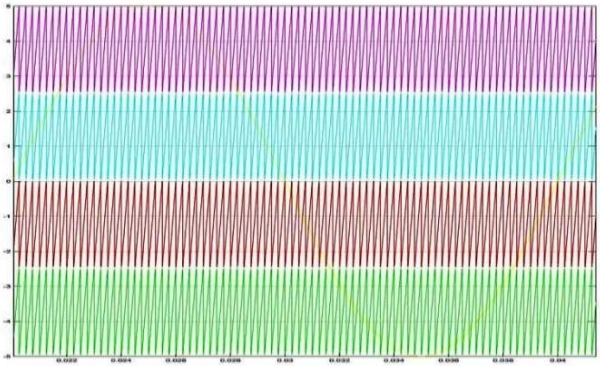

Fig .3. Phase Disposition PWM Technique

B. Phase Opposition Disposition (POD)

This technique employs a number of carriers (m-1) which are all in phase above and below the zero reference. In 5-level converters all the four carrier waves are phase shifted by 180 degrees between the ones above and below zero reference. The reference signal is compared with all four carrier waves thereby gate pulses are generated and are associated to each switching devices. The phase opposition disposition PWM technique is illustrated in Fig. 4.

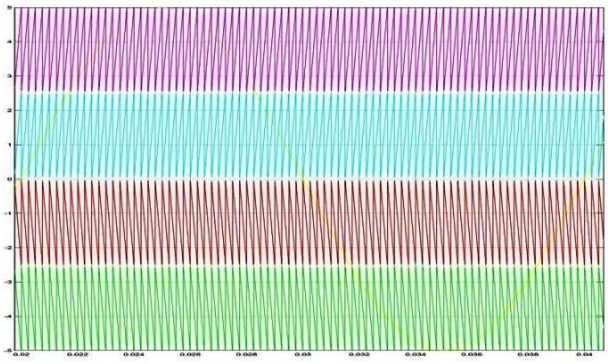

Fig .4. Phase Opposition Disposition PWM Technique

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1086-1091 ISSN: 2249-6645

C. Alternative Phase opposition Disposition (APOD)

This technique requires number of carriers (m-1) which are all phase displaced from each other by 180 degrees alternatively. The alternative phase opposition disposition PWM technique is illustrated in Fig. 5.

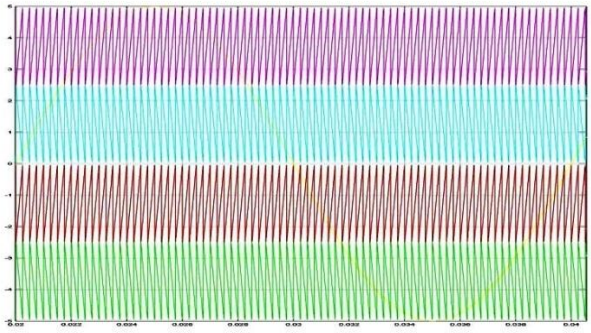

Fig .5. Alternative Phase opposition Disposition

D. Phase Shift (PS)

This technique employs a number of carriers (m-l) phase shifted by 90 degree accordingly. In 5 -level converter all the four carrier waves are phase shifted by 90 degree. The phase shifted PWM technique is illustrated in Fig. 6.

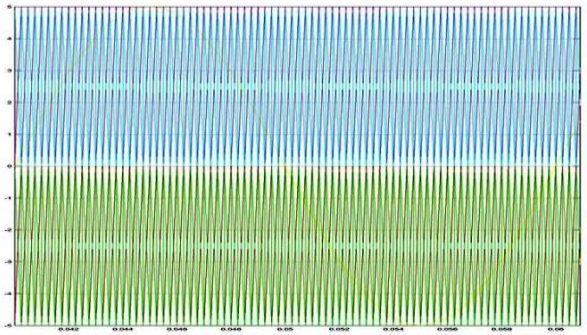

Fig .6. Phase Shifted PWM Technique

IV. SIMULATION AND EXPERIMENTAL RESULTS

The figure 7 shows the MATLAB/SIMULINK MODEL for 3-level neutral clamped multilevel inverter with PWM technique. It consists of 12 MOSFET switches, 6 clamping diodes and 2 DC link capacitors are connected with single DC source. The figure 10 shows the overall matlab/simulink model of three phase 5-Level neutral clamped multilevel Z-Source inverter. The figure 11 shows the subsystem diagram of 5-level neutral clamped multilevel inverter. This model consists of 24 MOSFET switches, 12 clamping diodes and 4 DC link capacitors with single DC source are connected in order to form 5-level neutral clamped multilevel Z-Source inverter. The figure 12 shows the multicarrier wave generation arrangement of the proposed converter. The figure 8 and 13 shows the output voltages of 3-level and 5-Level respectively. THD values of 3-level neutral clamped multilevel inverter with PWM technique as illustrated in Fig.9. THD values of different multicarrier PWM techniques are shown in figure 14 to 17. Experimental arrangement of neutral clamped multilevel z-source inverter is shown in figure 18.

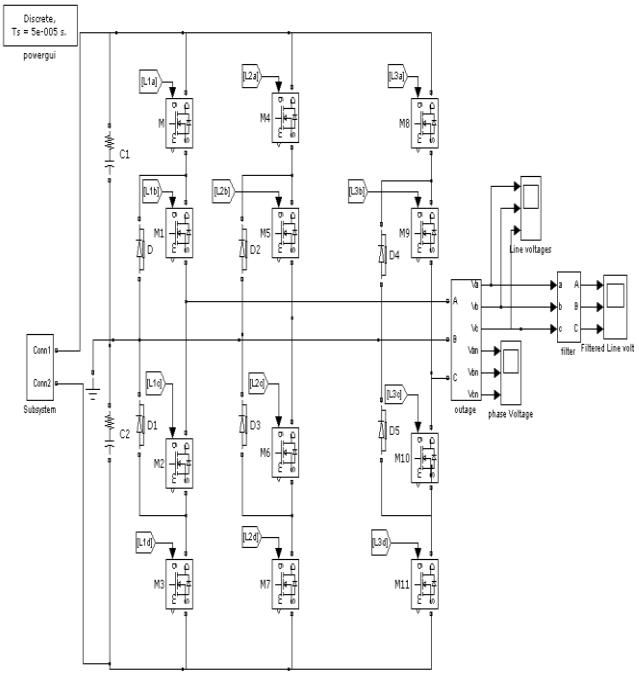

Fig .7. Three Phase 3-Level Neutral Clamped Multilevel Inverter Simulink Model

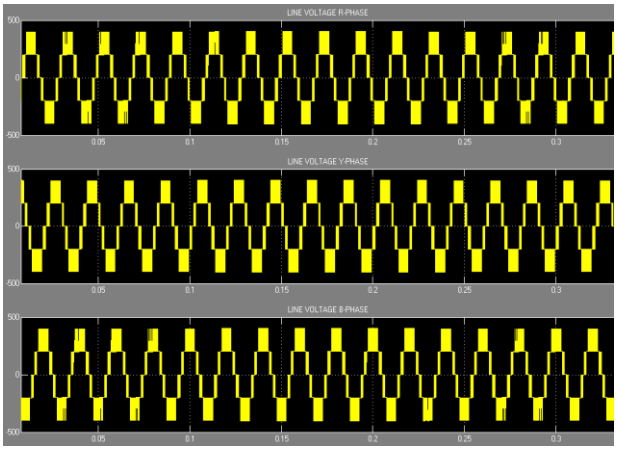

Fig. 8. Line Voltages of 3-Level Neutral Clamped Multilevel Inverter

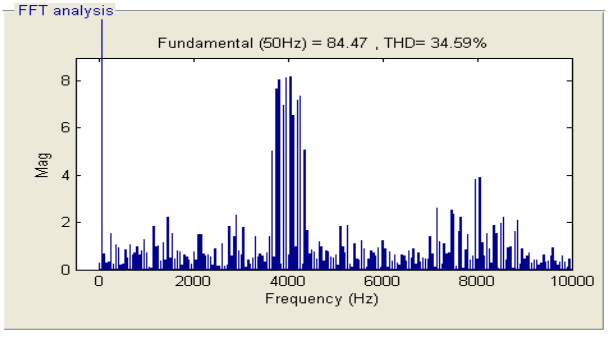

Fig .9. THD Values of 3-Level Neutral Clamped Multilevel Inverter with PWM Technique

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1086-1091 ISSN: 2249-6645

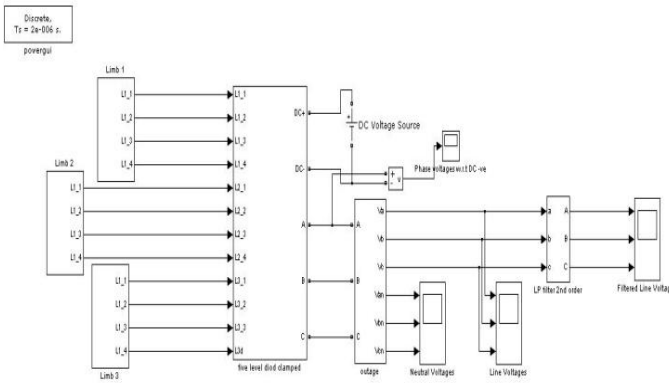

Fig .10. Three Phase 5-Level Neutral Clamped Multilevel Z-Source Inverter Simulink Model

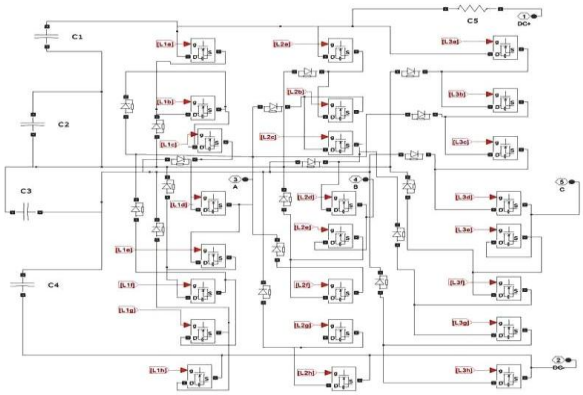

Fig .11. Subsystem Diagram of 5-Level Neutral Clamped Multilevel Inverter

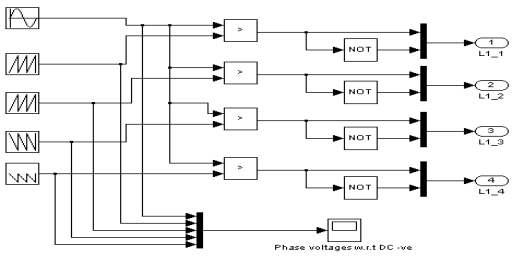

Fig. 12. Multicarrier Wave Generation

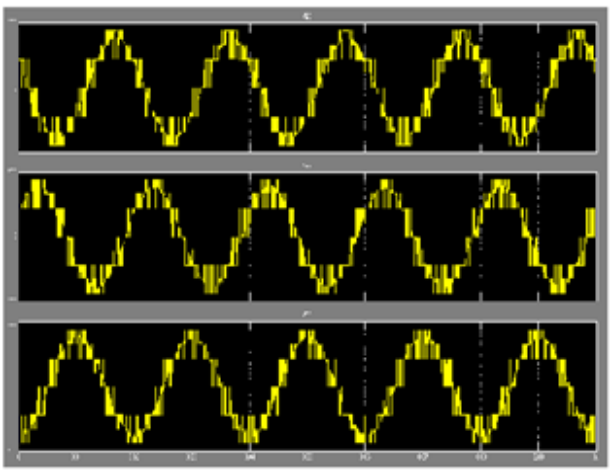

Fig.13. Line Voltages of 5-Level Neutral Clamped Multilevel Z-Source Inverter

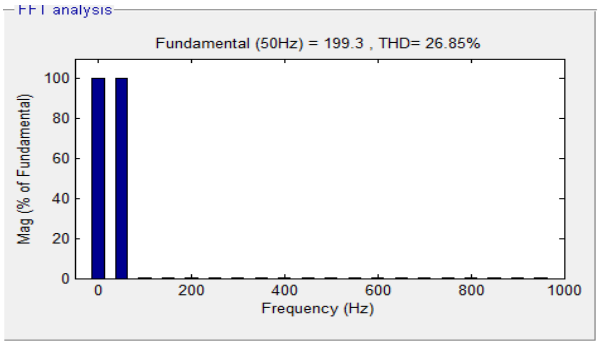

Fig .14. THD Values of Phase Disposition PWM Technique

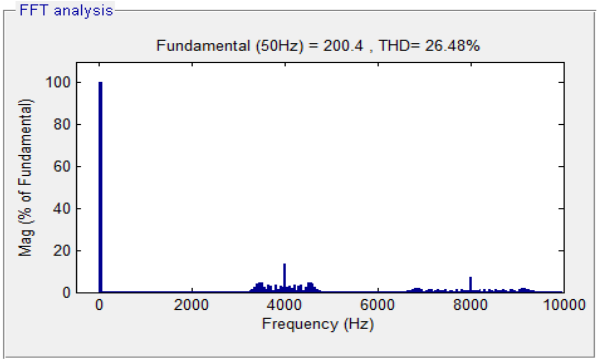

Fig .15. THD Values of Phase Opposition Disposition PWM Technique

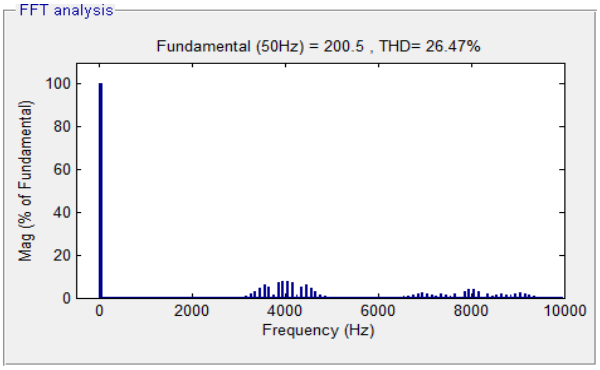

Fig .16. THD Values of Alternative Phase opposite Disposition PWM Technique

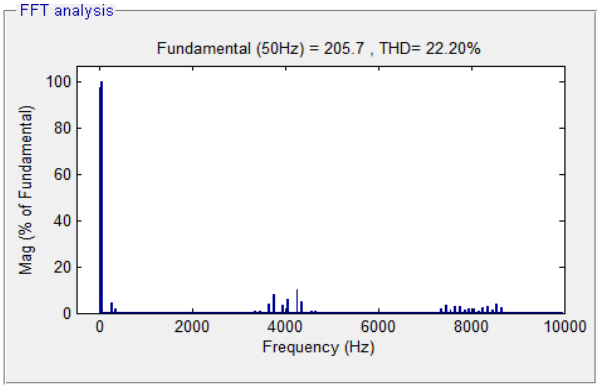

Fig .17. THD Values of Phase Shifted PWM Technique

Fig.18. Experimental Arrangement of Neutral Clamped Multilevel Z-Source Inverter

TABLE III
% OF THD VALUES

No of levels	Techniques	%THD
3-Level	PWM	34.59%
5-Level	Phase Disposition PWM	26.85%
	Phase Opposition Disposition PWM	26.48%
	Alternative Phase Opposite Disposition PWM	26.47%
	Phase Shifted PWM	22.20%

V. CONCLUSION

The comparative THD analysis of a three phase 5-level neutral clamped multilevel Z-source inverter is presented in this paper. The various multicarrier PWM technique like Phase disposition (PD), Phase opposition disposition (POD), Alternative phase opposition disposition (APOD) and Phase Shifted (PS) PWM techniques are applied to the proposed converter**.** The THD values of the output voltages are compared with all the above mentioned techniques. From the above discussion, it is absorbed that the phase shifted PWM technique has less harmonic content in the output phase voltage compared with other multicarrier PWM control techniques. The proposed work has compared to the conventional three level inverter with PWM technique by using MATLAB-SIMULINK.

ACKNOWLEDGEMENTS

The authors thank the Management, the Principal and EEE Department of Thiagarajar College of Engineering for providing the necessary facilities to carry out this work. Also the help and support of Management, the Principal and EEE department of Sri Subramanya College of Engg and Tech., during the course of this work is acknowledged

REFERENCES

[1] Poh Chiang Loh, Feng Gao, Frede Blaabjerg, and Sok weilim," Operational Analysis and Modulation Control of Three-Level Z-Source Inverters With Enhanced Output Waveform Quality," *IEEE Transaction On Power Electronics, Vol.24, No.7, July 2009.*

[2] Poh Chiang Loh, Feng Gao, Pee-Chin Tan, and Frede Blaabjerg," Three-Level AC–DC–AC Z-Source Converter Using Reduced Passive Component Count," *IEEE Transactions On Power Electronics, Vol. 24, No. 7, July2009.*

[3] Jing Zhao, Xiangning He and Rongxiang Zhao," A Novel PWM Control Method for Hybrid-Clamped Multilevel Inverters," *IEEE Transactions On Industrial Electronics, Vol. 57, No. 7, July 2010.*

[4] Brendan Peter Mcgrath and Donald Grahame Holmes," Multicarrier PWM Strategies for Multilevel Inverters," *IEEE Transactions on Industrial Electronics, Vol. 49,No.4, August 2002.*

[5] Samir Kouro, Pablo Lezana, Mauricio Angulo and José Rodríguez, "Multicarrier PWM With Dc-Link Ripple Feedforward Compensation For Multilevel Inverters," *IEEE Transactions on Power Electronics, Vol. 23, No.1, January2008.*

[6] Leon M. Tolbert, Fang Zheng Peng and Thomas G. Habetler," Multilevel PWM Methods At Low Modulation Indices," *IEEE Transactions on Power Electronics, Vol.15, No. 4, July 2000.*

[7] M. A. Saqib and S. A. R. Kashif," Artificial Neural Network Based Space Vector PWM for a Five-Level Diode-Clamped Inverter," *AUPEC, 2010.*

[8] Sreenivasarao D, Pramod Agarwal and B. Das," A Carrier- Transposed Modulation Technique for Multilevel Inverters," *PEDES, 2010.*

[9] S.Ebanezar Pravin and R.Narciss Starbell," Induction Motor Drive Using Seven Level MultilevelInverter for Energy Saving in VariableTorque Load Application,"*ICCCET March 2011.*

[10] P.T.Josh, Jovitha Jerome and Arul Wilson," The Comparative Analysis of Multicarrier Control Techniques For SPWM Controlled Cascaded H-Bridge Multilevel Inverter," Proceedings of *ICETECT 2011.*

[11] G.Durgasukumar and M.K.Pathak," THD Reduction Performance of Multi-Level Inverter fed Induction Motor Drive," *IICPC, 2011.*

S. MOHAMED YOUSUF was born in Tamil Nadu, India in 1985. He received B.E Electrical and Electronics Engineering from Sri Subramanya College of Engg and Tech, Palani, Dindigul (Dt) and M.E Power Electronics and Drives branch from PSNA College of Engg and Tech, Dindigul, Dindigul Dt, India. He is pursuing Ph.D. degree at Anna University, chennai, India. His area of interest is Power Electronics and Drives. He has published two papers in international journals, two papers in international conferences. He is currently working as a Assistant professor of Electrical and Electronics Engineering Department in Sri Subramanya College of Engg and Technology, Palani, Dindigul (Dt) Affiliated to Anna University. chennai, Tamilnadu, India.

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1086-1091 ISSN: 2249-6645

P. VIJAYADEEPAN was born in Tamil Nadu, India,in 1983. He received B.E Electrical and Electronics Engineering from Sri Subramanya College of Engg and Technology, Palani Dindigul (Dt) and M.E Power Electronics and Drives branch from PSNA College of Engg & Technology, Dindigul, Dindigul Dt, India. He is pursuing Ph.D. degree at Anna University, Chennai, India. His area of interest is Power Electronics and Drives. He has published two papers in international conferences. He is currently working as a Assistant professor of Electrical and Electronics Engineering Department in Sri Subramanya College of Engg and Tech, Palani, Dindigul (Dt) Affiliated to Anna University, chennai. Tamilnadu, India.

Dr. S. LATHA was born in Tamil Nadu, India, in 1965. She has completed Bachelor's degree in Electrical and Electronics Engineering on 1986 and Master's degree in Power Systems Engineering on 1987 from Thiagarajar College of Engineering, Madurai, India. She has completed Ph.D on November 2007 from Madurai Kamaraj University in the area of Flexible A.C Transmission System. She has been teaching for the past 20 years. She has secured first rank in Master's degree. She has published three papers in international journals, five papers in international conference. Her field of interest is application of Flexible AC Transmission System (FACTS) Controllers in Power System. She is currently working as a Associate professor of Electrical and Electronics Engineering Department in Thiyagarajar College of Engg, Madurai, India.