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CMOS Full Adders for Energy Efficient FIR Filters

Gayathri. K. K
ME student, Dept of EEE
Hindusthan College of Engineering and Technology
Coimbatore -641 032, India

Suresh Babu.A
Assistant professor, Dept of EEE
Hindusthan College of Engineering and Technology
Coimbatore-641 032,India

Abstract: *Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. We present two high-speed and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power-delay product (PDP). In this paper we are using CMOS full adders for the FIR filters. The adder element in the conventional FIR filter is replaced by the new CMOS full adder cells. So that the power consumption of the FIR filters can be reduced.*

Key words: *Adders,CMOS,FIR Filters, Low power,VLSI*

I. INTRODUCTION

Addition is one of the fundamental arithmetic operations. It is used in extensively in many of the VLSI systems such application specific DSP architectures, microprocessors etc...Adder is the core component of an arithmetic unit. The efficiency of the adder determines the efficiency of the arithmetic unit .Various structures have been evolved trying to improve the performance of the adder in terms of area, power and speed. Full adders is the core of many arithmetic operations such as addition, subtraction, multiplication, division and address generation. The PDP exhibited by the full adders would affect the system's overall performance. There
are three major components of power dissipation in complementary metal oxide(CMOS) circuits: switching power, short circuit power and static power. Reducing any of these components will end up with low power consumption of the whole system[2].

A filter is used to modify an input signal in order to facilitate further processing. FIR digital filters have many excellent features such as the stability, easiness for realization, and suitable to be used to design multi-pass band or multi-stop band digital filters. Filter consists of mainly three elements, adders, multipliers and delay elements. This paper describes the design and performance comparison of two full adder cells implemented with an alternative internal logic structure that is based on the multiplexing of the Boolean functions XOR/XNOR and AND/OR , to obtain the sum and the carry outputs respectively. These CMOS full adders are used as adder elements for the design of FIR filters.There was a pass transistor powerless/groundless logic structure to reduce the power consumption.

II. PREVIOUS WORKS

Several papers have been published regarding the power optimization of low power full adders. Even more , some works have presented intense comparisons between different full adder schemes.The different logic styles such asstandard CMOS, differential cascade voltage swing restored CPL(SR-CPL) and hybrid styles are used to build the adder modules.

The internal logic structure shown in Fig. 1. has been adopted as the standard configuration in most of the enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate to obtain A XOR B and A XNOR B and multiplexers to obtain the SUM (*So*) and CARRY (*Co*) outputs. The major problem regarding the propagation delay for a full-adder is that it is necessary to obtain an intermediate A XOR B signal and its complement ,which are then used to drive other blocks to generate the final outputs. Thus, the overall propagation delay and, in most of the cases, the power consumption of the full-adder depend on the delay and voltage swing of the signal and its complement generated within the cell. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path.

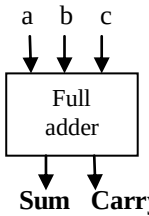

Fig1.Block of full adder

a)Conventional CMOS Style

A basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and Cin) and two 1-bit outputs (*sum* and *carry*). The relations between the inputs and the outputs are expressed as[7];

$sum = (a \text{XOR} b) \text{XOR} c$

$carry = a \times b + c \times (a \text{XOR} b)$

The above Boolean expressions may be rearranged as:

$sum = c\,(a + b + c) + a \times b \times c$

$carry = a \times b + c \times (a + b)$

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III. ALTERNATIVE LOGIC STRUCTURE FOR A FULL-ADDER

The truth table for 1 bit full adder is shown in the table1. Examining the full-adder's true-table , it can be seen that the *So* output is equal to the A XOR B value when C=1 and it is equal to A XNOR B when C=0. Thus, a multiplexer can be used to obtain the respective value same criteria, the *Co* output is equal to the A AND B value when C=0, and it is equal to value when A XOR B. Again, C can be used to select the respective value for the required condition, driving a multiplexer[8]. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the A XOR B and A XNOR B signals, another block to obtain the A AND B and A OR B signals, and two multiplexers being driven by the C_{in} input to generate the *So* and *Co* outputs, as shown in Fig. 1

The features and advantages of this logic structure are as follows[10].

• There are not signals generated internally that control the selection of the output multiplexers. Instead, the c input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.

• The capacitive load for the c input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the signal falls on the critical path can be reduced.

• The propagation delay for the *So* and *Co* outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wavepipelining),and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.

• The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NORgates at the input of the multiplexers, improving in this way the performance for load-sensitive applications.

Truth table for full adder

C	B	A	S_0	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1:- Truth table for full adder

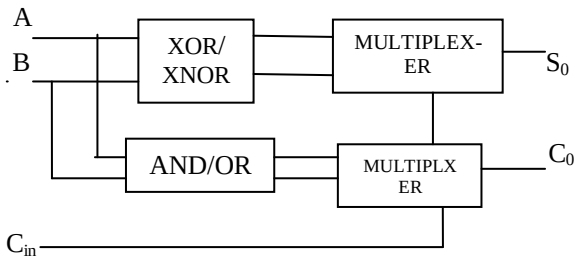

Fig 1: *An alternate logic scheme for full adders[10]*

A full adder consists of two XOR gates, three AND gates and one OR gate. These gates are used for obtaining the sum and carry outputs.

IV. FIR Filters

FIR means Finite Impulse Response filters. If the response of the system is of finite duration , then the system is called Finite Impulse Response systems. FIR digital filters have many excellent features such as the stability, easiness for realization, and suitable to be used to design multi-passband or multi-stopband digital filters, which makes it widely used in communication, radar, biomedical as well as automation fields. FIR filters specification include the maximum tolerable pass band ripple, maximum tolerable stop band ripple, pass band edge frequency and stop band edge frequency.

An FIR filter has a number of useful properties which sometimes make it preferable to an Infinite Impulse Response(IIR) filter. FIR filters:

- Require no feedback. This means that any rounding errors are not compounded by summed iterations. The same relative error occurs in each calculation. This also makes implementation simpler.
- Are inherently stable. This is due to the fact that, because there is no required feedback, all the poles are located at the origin and thus are located within the unit circle (the required condition for stability in a Z transformed system).
- They can easily be designed to be linear phase by making the coefficient sequence symmetric; linear phase, or phase change proportional to frequency, corresponds to equal delay at all frequencies. This property is sometimes desired for phase-sensitive applications, for example data communications.

The main disadvantage of FIR filters is that considerably more computation power in a general purpose processor is required compared to an IIR filter with similar sharpness orespecially when low frequency (relative to the sample rate) cutoffs are needed. However many digital signal processors provide specialized hardware features to make FIR filters approximately as efficient as IIR for many applications.

FIR filters consists of three elements; adder, multliplier and delay elements. Fig 3 shows the schemetic diagram of FIR filter of order L[11]

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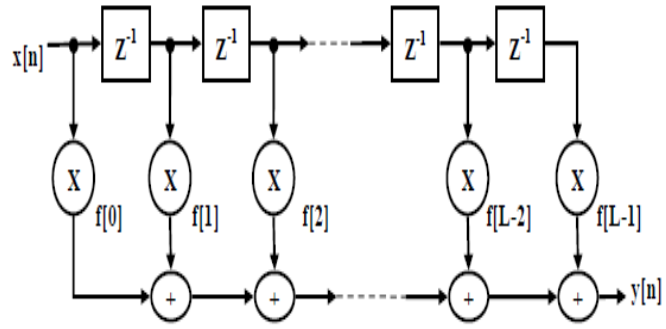
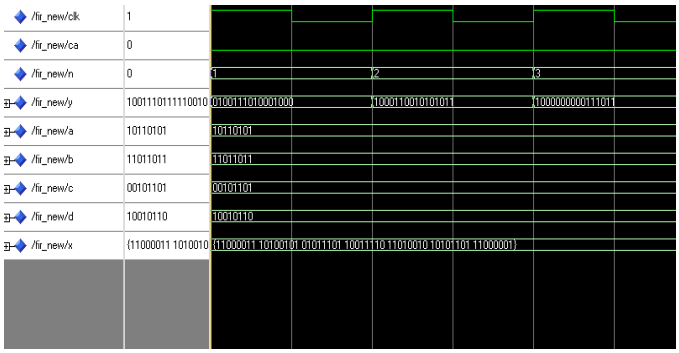


Fig 3.Schematic diagram of FIR filter of order L

V. IMPLEMENTATION



The adder elements in the FIR filters can be replaced by the low power CMOS full adders. So that the total power dissipation of the FIR filters is reduced. The power consumption of the filters can be find out by using the Xilinx software. The FIR filters can be simulated in the Modelsim ISE.

VI. RESULTS

The power, delay and area can be analyzed by using the Xilinx software. PDP value is the product of power and delay of the full adder cells. The comparison between the conventional full adder and the proposed full adder is shown in the table below.

Parameters	Conventional full adder	Proposed full adder
Power	123mw	67mW
Delay	7.989ns	7.476ns
No: of gates	36	12
PDP	982.65Ws	590.604Ws

Table 2: comparison between conventional and proposed full adders.

The new FIR filter will have low power consumption than the conventional FIR filters. The power consumption of the new FIR filters can be reduced up to 60% than the conventional full adders. The developed CMOS full adders can be implemented in the FIR Filters. So that the power consumption and delay can be reduced . Thus the overall performance of the FIR filters can be increased. The comparison table of different FIR filters are shown in the table3.

FIR FILTERS	POWER CONSUMPTION	DELAY
4tapped conventional FIR Filters	154mW	3.584ns
4tapped new FIR Filters	147mW	3.014ns
8tapped conventional FIR Filters	161mW	4.587ns
8tapped new FIR Filters	152mW	3.152ns
16tapped conventional FIR Filters	175mW	4.654ns
16tapped new FIR Filters	162mW	3.225ns

Table 3: Comparison of different FIR filters.

VII. CONCLUSION

An alternative internal logic structure for designing full-adder cells was introduced. The full adder was designed using the multiplexing of XOR/XNOR gates and AND/OR gates.The full adders are designed using Xilinx software.The speed, power and area of the designed system is analysed by using the Xilinx software.

PDP is the main factor which determines the performance of the system. Power delay product is a quantitative measure of the efficiency of the trade off between power dissipation and speed, and is particularly important when low power operation is needed. The power consumption of the new full adders is reduced up to 60%. The delay of the full adder is also reduced . Thus the power delay product(PDP) of the proposed full adders have an advantage of 60%. Thus the over all performance of the full adder is improved. By using this type of full adders in the arithmetic modules of the FIR filters the power consumption can be reduced and hence the overall performance of the system can be improved.

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