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Design and Implementation of Date Rate Controller Using Micro blaze Processor

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Abstract: - FPGA-based solutions become more common in embedded systems these days. These systems need to communicate with external world. Considering high-speed and popularity of Ethernet communication, developing a reliable real-time Ethernet component inside FPGA is of special value. The Ethernet Mac (Media access control), sub level with in data link layer of the OSI reference model. Ethernet performance has increased from megabits per second (M bits/s) to gigabits per second (G bits/s) and its popularity reflects not only its status as an IEEE standard, but because the Ethernet protocol has a number of features and benefits that have proved attractive to designers and engineers. The Mac is the portion of the Ethernet core that handles transmitting and reception of the frames. It performs the frames data encapsulation and de-capsulation, frame transmission and frame reception. In this paper the authors presented up to the data rate transmission from a PC to FPGA board and the work is carried out in XILINX10.1 EDK tool in C language.

Keywords **– EDK, FPGA, MAC, OSI, Microblaze processor.**

I. INTRODUCTION

FPGAs are increasingly being used for many systems and efficient SoC (System-on-a-Chip) designs. Competitive market environment and high security areas such as military systems are among the factors that make protecting designs implemented in FPGAs more important. Without proper safeguards, design information and proprietary intellectual properties face major security risks and attackers will be able to steal the design contained in the bit stream of FPGAs. In common with earlier IEEE 802.3 standards, 10 Gigabit Ethernet will ultimately define a standard which ensures interoperability between products from different vendors. The standard primarily specifies the physical layers and only a small change will be made to the media access control (MAC). [1][3]The adoption of cost effective, robust technologies largely enabled Ethernet to dominate the LAN market; the same approach is being used in the development of the 10 Gigabit Ethernet (10GbE). A significant difference however is that 10GbE represents the merging of data communications and telecommunications. In the International Standards Organization's Open Systems Interconnection (OSI) model, Ethernet is fundamentally a Layer 2 protocol. 10 Gigabit Ethernet uses the IEEE 802.3 Ethernet Media Access Control (MAC) protocol, the IEEE 802.3 Ethernet frame format, and the minimum and maximum IEEE 802.3 frame size. Just as Gigabit Ethernet remained true to the Ethernet model, 10 Gigabit Ethernet continues the natural evolution of Ethernet in speed and distance. Since it is a full-duplex only and fiber-only technology, it does not need the carrier-sensing, multiple-access with collision detection, (CSMA/CD) protocol that defines slower, half-duplex Ethernet technologies. In every other respect, 10 Gigabit Ethernet remains true to the original Ethernet model.

An Ethernet PHYsical layer device (PHY), which corresponds to Layer 1 of the OSI model, connects the media to the MAC layer, which corresponds to OSI Layer 2. Ethernet architecture further divides the PHY (Layer 1) into a Physical Media Dependent (PMD) and a Physical Coding Sublayer (PCS). Optical transceivers, for example, are PMDs. The PCS is made up of coding (e.g., 64/66b) and a serialize or multiplexing functions. the following figure shows the architecture of the data flow from physical layer to the data link layer.[5]

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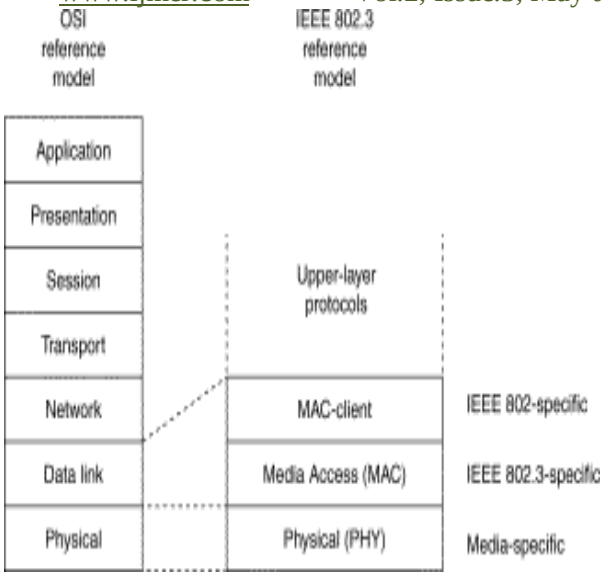

Fig 1. Layer representation of LAN Model with respective to OSI reference model.

The combination of the physical coding sub layer (PCS), the physical medium attachment (PMA), and the physical medium dependent (PMD) sub layers consists the physical layer protocol.

II. ABOUT LAN

Ethernet is the most widely-installed local area network (LAN) technology. Specified in a standard, IEEE 802.3, Ethernet was originally developed by Xerox from an earlier specification called *Alohanet* (for the Palo Alto Research Center Aloha network) and then developed further by Xerox, DEC, and Intel. An Ethernet LAN typically uses coaxial cable or special grades of twisted pair wires. Ethernet is also used in wireless LANs. The most commonly installed Ethernet systems are called 10BASE-T and provide transmission speeds up to 10 Mbps. Devices are connected to the cable and compete for access using a Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. Fast Ethernet or 100BASE-T provides transmission speeds up to 100 megabits per second and is typically used for LAN backbone systems, supporting workstations with 10BASE-T cards. Gigabit Ethernet provides an even higher level of backbone support at 1000 megabits per second (1 gigabit or 1 billion bits per second). 10-Gigabit Ethernet provides up to 10 billion bits per second.[5]. The frame format for the Ethernet is given below in which the data is transmitted in between the physical medium and the data link layer medium.

PRE	SOF	DA	SA	Type	Data	FCS
7	1	6	6	2	1500	4

Fig 2: Ethernet frame structure.

The following gives the detailed description of the parameter used in the Ethernet frame structure.

PRE(Preamble) : it is of 7byte and is an alternating patterns of 1`s and 0`s that tells receiver stations that a frame is coming and that provides a means to synchronize the frame reception portions physical layer with incoming bit stream.

SOF(Start of frame delimiter) : it is of 1 byte, and an alternating patterns of 1`s and 0`s ending with two consecutive 1-bits indicating that the next bit is the left most bit in the left most byte of destination address.

DA(destination Address) : it is of 6 bytes indicating the which station should receive the frame.

SA(sending Address) : it is of 6 bytes indicating the which station should sends the frame.

LENGTH/TYPE: it is of 2 bytes, this field indicates either the number of the MAC client data bytes that are contained in the data filed of the frame of the frame type ID if the frame is assembled using an optional format.

DATA : it is a sequence of ‘n’ bytes (46<=n<=1500) of any value of total frame with 64 bytes.

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FCS(Frame check sequence) : it is of 4bytes contains 32-bit crc value which is creates by the sender MAC and is re-calculated by the recovering MAC to the check for damage format.

III. CYCLIC REDUNDANCY CHECK

The cyclic redundancy check is a technique for detecting errors in digital data, but not for making corrections when the error are detected. It is used primarily in data transmission. In CRC a certain number of check bits, often called check sum are appended to the message being transmitted. The receiver can determine whether or not the check bits agree with the data to ascertain with a certain degree of probability whether or not an error occurred in transmission. If an error occurred the receiver sends a –ve acknowledgement back to the sender, requesting that the message be re transmitted. The technique is also some times applied to the data storage devices, such as disk drives. In this situation each block on the disk would have check bits and the hardware might automatically initiate a re-thread of the block when the error is detected , or it might report the error to software . the material that follows speaks in terms of a 'sender' and a 'receiver' of a message but it should be under stood that it applies to storage writing and reading. Theory of CRC is straight forwarded, the data is treated by the CRC algotrithm as a binary number[8]. This number is divided by another binary number called the polynomial. The rest of the division is the CRC check sum which is appended to the transmitted message . the receiver divides the message by the same polynomial the transmitted used. If the result of this addition is zero then the transmission was successful. However if the result is not equal an error occurs during transmission. CRC is a common method for detecting errors in transmitted messages or stored data. The CRC is a very powerful but easily implemented technique to obtain data reliability.

IV. MICROBLAZE ARCHITECTURE

Micro blaze is a 32-bit RISC Harvard soft core processor that can be embedded in the re-configurable logic of an fpga.The fixed feature set of the processor includes:

• 32-bit general purpose registers

• 32-bit instruction word with three operands and two addressing modes

• 32-bit address bus

• Single issue pipeline

• Having up to 14 special purpose registers.

The micro blaze core is parameterized to allow enabling of a set of configurable features. The micro blaze is having an extensive instruction set with many of a operations having large number of variants for registers, immediate, const, signed and unsigned[6][5]. The basic design can be configured with advances features such as barrel shifter, memory management unit, floating point, caches, exception handling and debug logic. In addition some of the logics such as floating point multiplication and division are optional in various hardware configurations. Micro blaze soft core processor is a major component of XILINX EDK. The EDK also includes the XPS(Xilinx Platform Studio) and a library of peripheral Ip soft cores. The Micro blaze architecture is shown below. Designing a microblaze embedded processor with multiple peripherals using both vendor supplied and the user created custom IP`s each of which has a different level of priority.

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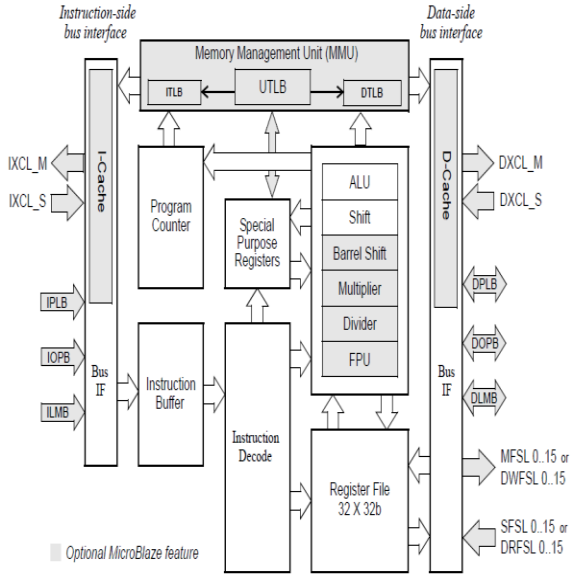

Fig3. Micro blaze Architecture.

V.EXPERIMENTALSETUP AND RESULTS

The main aim of this paper is to show that even we can create a web server application basing on the SPARTAN xc3s500e FPGA. There are certain adjustments that should be done in the XILINX10.1 EDK tool to get the data rate controlling in between the PC and the FPGA Board. This paper only provides up to some extend where the data is transferred and received by the board i.e.., through physical medium and data link layer using MAC`s sub portion layers and establishing a connection between FPGA and regular PC. There are two more libraries that to be included in the XILINX EDK project they are XILMFS [XILINX MEMORY FILE SYSTEM] and LWIP [Light weight IP]. The LWIP is again having 5 more sub libraries to modify as they are

- TFTP server.
- ECHO server.
- WEB server.
- TCP Rx through put test.
- TCP Tx through put test.

After initializing the above mentioned libraries which are available in ‘software’ and ‘software setting libraries as shown in the below two figures.

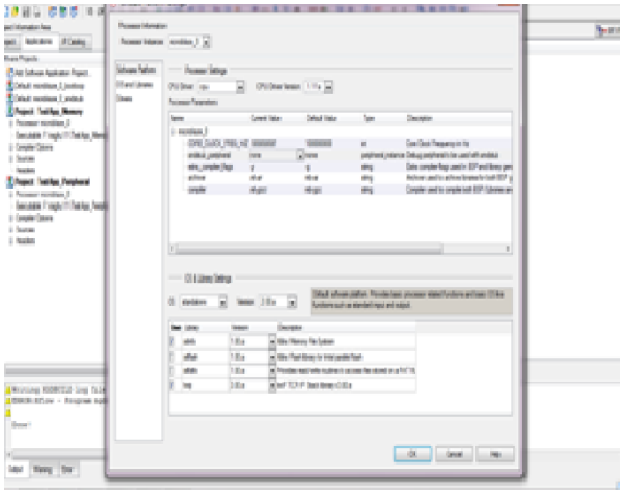

Fig 4 Adding XILMFS to the existing EDK project.

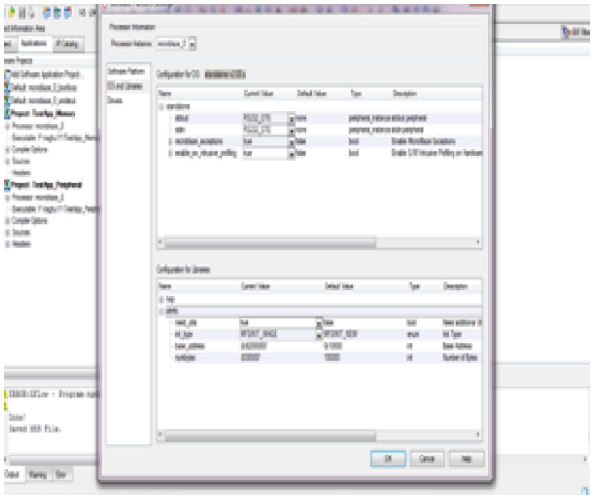

Fig 5 Adding LWIP to the existing EDK Project.

The code is written in C language for the web server application and we check for the details of the MAC and then we go for the output results. The experimental set up for this paper is shown in the below figure.

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Fig6 Experimental set up SPARTAN 3E board.

First we verify the MAC layers which is a sub portion of the physical layer and data link layer.

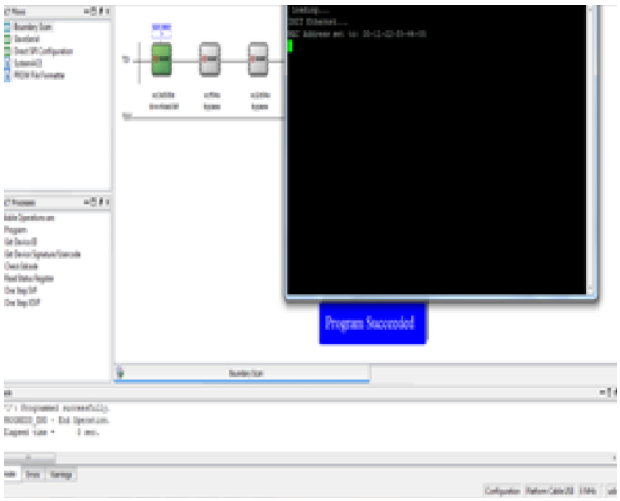

Fig 7 testing MAC layers.

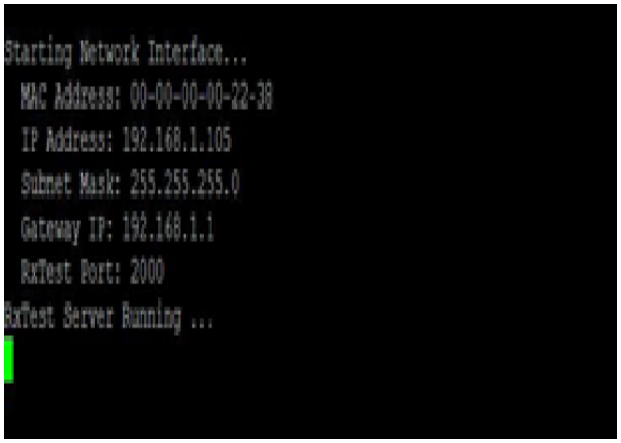

Fig8 PC and FPGA board are pinged with each other.

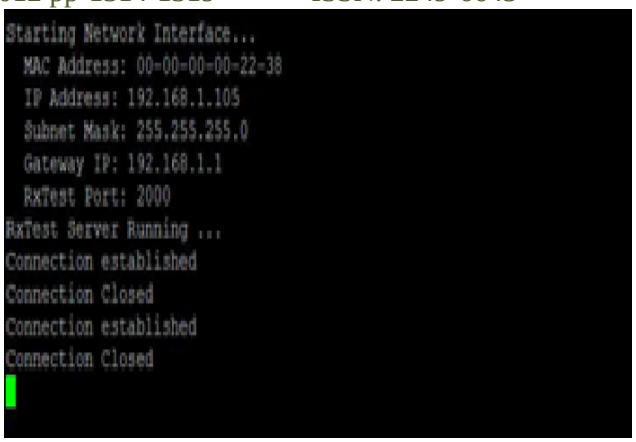

Fig9 connection established and closed.

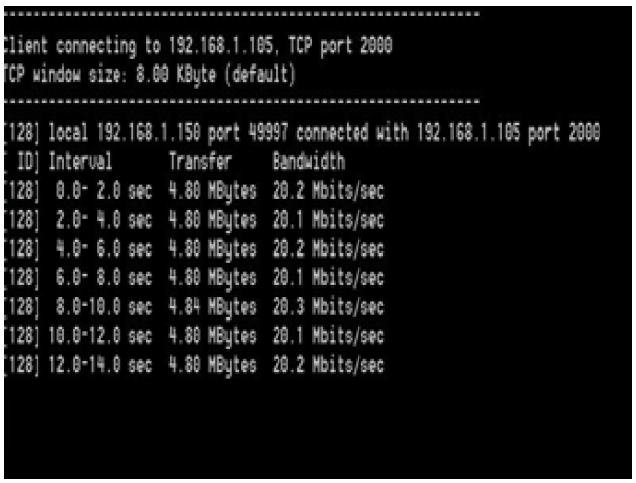

Fig 10 data rate transmission between FPGA board and PC.

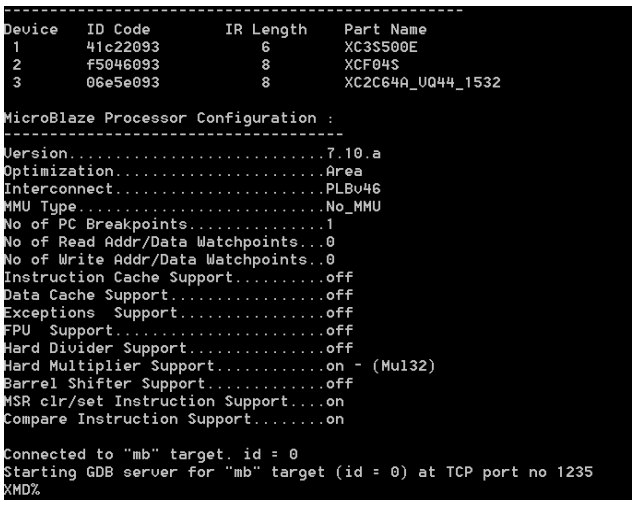

Fig11. TCP/IP connected with the local host or the targeted device

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The above results all are verified in the putty terminal using the cross over Ethernet cable. Hence we can say that by using a microblaze processor we can access the data flow between two peripherals.

VI. CONCLUSION

The Ethernet is intended primarily for use in such areas as office automation, distributed data processing, terminal access, and other situations requiring economical connection to a local communication medium carrying bursty traffic at high peak data rates. Hence we can conclude that the web server application can be possible by using SPARTAN 3E fpga and we can monitor the other peripherals which are presented on the FPGA board but require time to initialize that application.

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