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Optimal Design of CMOS OP-AMP VIA Geometric Programming

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Abstract: **In this paper a new method for determining the component values and transistor dimensions for CMOS operational amplifiers (Op-Amps) is presented. As a wide variety of design objectives and constraints are Posynomial function of the design variables, the Optimization is done by Geometric Programming. As a consequence we can efficiently determine globally optimal trade-offs among competing performance measures such as power, open-loop gain and bandwidth. In this paper I applied this method to a Folded Cascode operational amplifier. The paper shows how the method can be used to synthesize robust design, i.e., design guaranteed to meet the specifications for a verity of process condition and parameters. The synthesis method is fast and determines the globally optimal design.**

Keywords: Op-amp, Geometric Programming

I. INTRODUCTION

In response to the ever increasing demands of mixed mode integrated circuits, a variety of techniques have been developed for the efficient sizing of the CMOS op-amp circuits. One possible solution for this is to use Geometric Programming in convex form with which the globally optimal solution can be computed with great efficiency [2]. The performance measures such as input-referred noise, output voltage swing, unity-gain bandwidth, open-loop voltage gain common-mode rejection ratio, slew rate and so on are determined by the design parameters, e.g., transistor dimension, bias current and other component values. By Geometric Programming we can determine values of the design parameters that optimize an objective measure while satisfying specification or constraint on the performance measures [3]. There are other approaches also for the designing of op-amp e.g., classical optimization methods, knowledge-based methods, or global optimization methods. Classical Optimization methods such as steepest descent, sequential quadratic programming and lagrange multiplier methods have been widely used in analog circuit CAD. The main disadvantage of the classical optimization methods is that they only find locally optimal design and also can fail to find a feasible design. Classical methods tend to slow down if complex models are used [5]. On the other hand knowledge-based methods find locally optimal design instead of globally optimal design and the final design depends on the initial chosen parameters also the substantial human intervention is required during the design or training process. Global optimization methods such as branch and bound and simulated annealing are widely used in analog circuit design that guaranteed to find the globally optimal design. As with the other approaches both branch and bound and simulated annealing suffers from the slow speed and cannot guarantee a global optimal solution. In the comparison of other approaches the most important feature of geometric programming is that the globally optimal solution can be computed with great efficiency, even for the problems with hundreds of variables and thousands of constraints, using recently developed interior-point algorithms. By means of geometric programming infeasible specifications are unambiguously recognized i.e. the algorithm either produce a feasible point or a proof that the optimization procedure is completely irrelevant. The method can be used to simultaneously optimize the design of a large number of op-amps in a single large mixed mode integrated circuit. Another application is to use the efficiency to obtain robust design. In particular since the global optimum is found, the op-amps designed are not just the best this method can design, but the best any method can design [1].

In this novel work folded-cascode op-amp is designed with the help of Geometric Programming. The simulation results obtained from the MATLAB i.e., the width and the length of all transistors, are used for the spice verification.

II. FOLDED-CASCODE OP-AMP DESIGN

The designing of the folded cascade op-amp shown in Fig.1 is done using ggplab toolbox in the MATLAB [4]. The performance specifications and constraints like symmetry and matching, device sizing, area, bias conditions, common mode input range, output voltage swing, gate overdrive, quiescent power, open loop gain, slew rate and gain bandwidth are expressed as posynomial functions and posynomial constrained so automated design is done with sensitivity analysis via geometric programming [6]. The simulation results obtained from the MATLAB i.e., the width and the length of all transistors, are used for the spice verification.

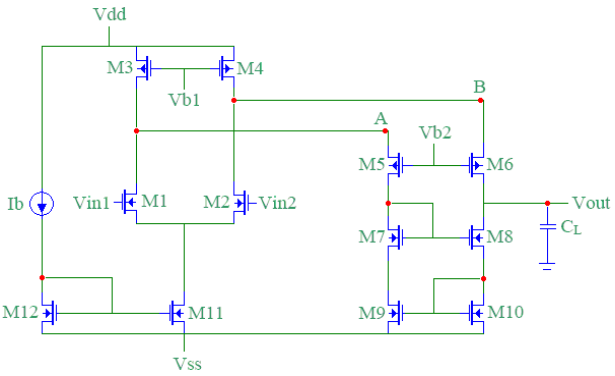

Fig. 1. Folded-Cascode op-amp

On the basis of simulation results, the optimised parameters for the designed circuit are given in table.1:

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Variable	Value	Unit
Ib	24.6	µA
W_1 / L_1	40 / 1	µ / µ
W_2 / L_2	40 / 1	µ / µ
W_3 / L_3	80 / 1	µ / µ
W_4 / L_4	80 / 1	µ / µ
W_5 / L_5	80 / 1	µ / µ
W_6 / L_6	80 / 1	µ / µ
W_7 / L_7	40 / 1	µ / µ
W_8 / L_8	40 / 1	µ / µ
W_9 / L_9	40 / 1	µ / µ
W_{10} / L_{10}	40 / 1	µ / µ
W_{11} / L_{11}	80 / 1	µ / µ
W_{12} / L_{12}	20 / 1	µ / µ

Table. 1.Optimal design points for the folded cascode op-amp

III. RESULTS AND DISCUSSION

Simulation results obtained from the MATLAB i.e. Width and Length of all transistors are used for the spice verification. The proposed design has been simulated and verified using spice. Spice simulation results using optimal design point variables against various given specifications are shown in Table.2. Spice simulation graphs are also shown for low frequency gain Fig.2, slew rate Fig.3, phase margin Fig.4, output swing Fig.5 and common mode gain Fig.6.

Performance measure	Specification	Spice simulation
Gain (dB)	≥ 60	76
Unity-gain BW (MHz)	≥ 5	55
	≥ 60	89
Phase margin (^{0})	≤ 5	1.6
Power (mW)	-3, 3	-2.2, 2.4
Output swing (V)	≥ 10	63
Slew rate (V/µs)	≥ 60	95
CMRR (dB)	-	8.5
BW (KHz)		

Table. 2.Spice simulated results for folded cascode op-amp

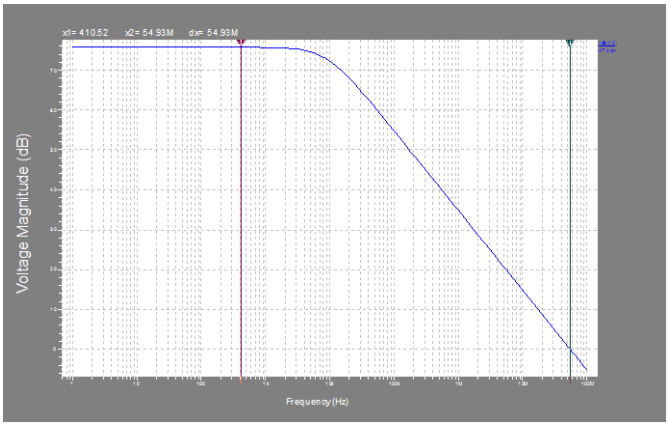

Fig. 2. Low Frequency Gain

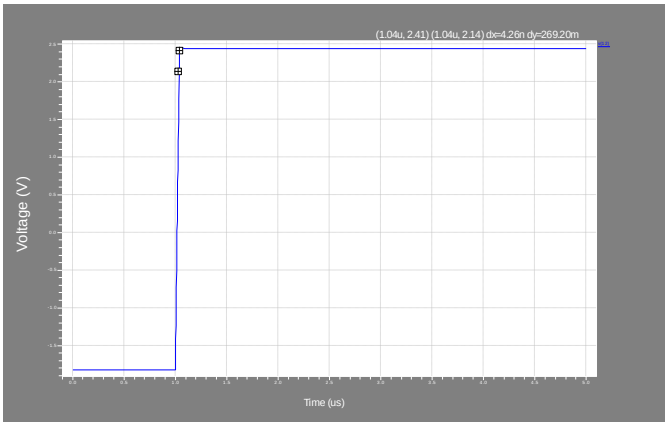

Fig. 3. Slew rate

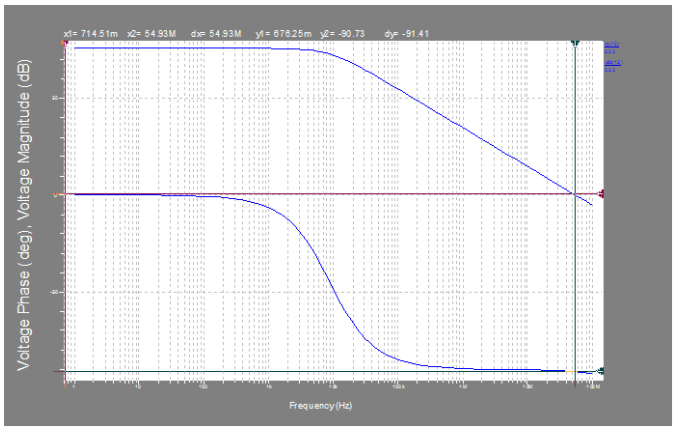

Fig. 4. Phase margin

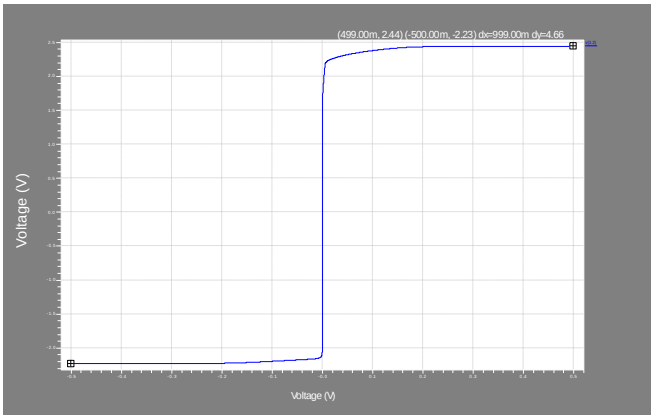

Fig. 5. Output swing

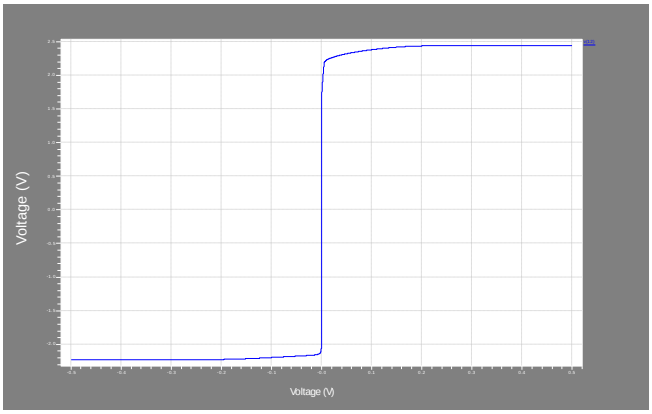

Fig. 6. Common mode Gain

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IV. CONCLUSIONS

The method yields globally optimal design, is extremely efficient and handles a wide variety of practical constraints. The method could be used to do full custom design for each op-amp in complex mixed signal integrated circuit. The method unambiguously determines feasibility of a set of specifications, or it provides a proof that the specification cannot be achieved. The main disadvantage of the method is that it handles only certain types of constraints and specifications, i.e., monomial equality constraints and posynomial inequality constraints, despite this apparently restricted form, we can handle a very wide variety of practical amplifier specifications.

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